ME-906

project
mercury

HANDBOOK OF INSTRUCTIONS FOR MEC MODEL 75 DATA RECEIVER

prepared for
National Aeronautics and Space Administration
Contract No. NAS 1-430

30 November 1960
Revised 15 June, 1962

Milgo Electronic Corporation
for
International Business Machines Corporation

in association with

WESTERN ELECTRIC COMPANY, INC.

LIST OF EFFECTIVE PAGES

TOTAL NUMBER OF PAGES IS 141, AS FOLLOWS:

Page No.	Issue
Title Page	Rev. 6/12/62
*List of Effective Pages	Rev. 6/12/62
i and ii	Original
iii	11 Aug. 61
iv	Original
1-1	Original
2-1 thru 2-3	Original
3-1	Original
*3-2	Rev. 4/18/62
3-3 and 3-4	11 Aug. 61
3-5 and 3-6	Original
*3-7 thru 3-10A	Rev. 4/18/62
3-11	11 Aug. 61
3-12	Original
3-13 and 3-14	11 Aug. 61
3-15	Original
3-16	11 Aug. 61
3-17 and 3-18	Original
4-1 and 4-2	Original
*4-3 and 4-4	Rev. 4/18/62
5-1	Original
6-1	Original
*Parts List	Rev. 6/12/62
*Wire List	Rev. 4/18/62
9-1 and 9-2	Original
9-3A	11 Aug. 61
*9-3B	Rev. 4/18/62
9-4 thru 9-8	Original
*9-9A thru 9-9B	Rev. 6/12/62
9-10 thru 9-14	Original
*9-15 and 9-16	Rev. 4/18/62
*9-17 and 9-18	Rev. 4/18/62
9-19 thru 9-26	Original
9-27	Original
Appendix Title Page	Original
Page 1 and 2 of 12	Original
Page 3 of 12	11 Aug. 61
Page 4 thru 12 of 12	Original
Page 1 thru 7 of 7	Original
Page 1 thru 8 of 8	Original
Page 1 thru 3 of 3	Original
Page 1 thru 3 of 3	Original
Page 1 and 2 of 2	Original
Page 1 and 2 of 2	Original
Page 1 and 2 of 2	Original
Page 1 thru 3 of 3	Original
Page 1 and 2 of 2	Original
Page 1 and 2 of 2	Original

*The asterisk indicates pages changed, added or deleted by the current change.

TABLE OF CONTENTS

LIST OF ILLUSTRATIONS

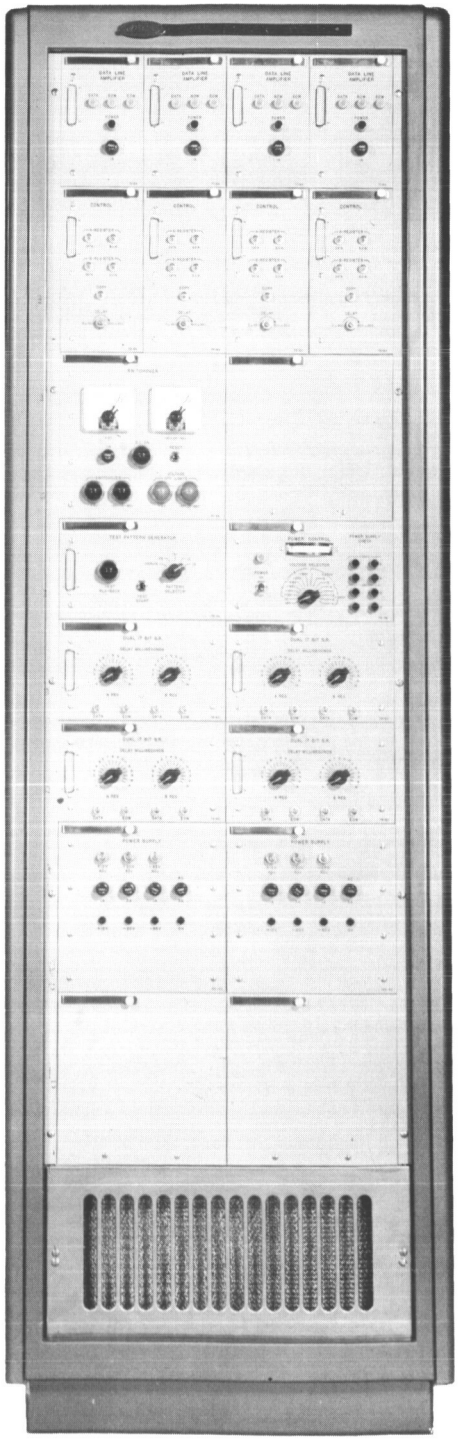


Figure 1-1. MEC Model 75 Data Receiver

CHAPTER I

INTRODUCTION

1-1. PURPOSE OF EQUIPMENT (Figure 1-1)

1-1.1. The MEC Model 75 Data Receiver accepts four channels of data which have been transmitted over telephone voice lines, with time displacement, by MEC Model 74 Data Transmitter. These four channels may have various delays with respect to one another as determined at the transmitting site, with the limitation that the maximum delay does not exceed 16 milliseconds. The data arrives via four separate routes and will encounter additional delays of various amounts depending upon the types of transmission equipment used enroute. Misalignment of the data is done in order to lessen the possibility of external noise affecting all data lines in a like fashion once it leaves the source.

1-1.2. Data is also accepted from a MEC Model 1585-1A Tape Recorder. The Receiver aligns the time displaced data and has outputs to MEC Model 76 500 Bit Receiver. These outputs consist of four pair of data lines, four pair of copy lines, and four pair of End-of-Word (EOW) lines, all of which contain identical information. There are also four outputs which provide data that has been filtered and amplified to MEC Model 1585-1A Tape Recorder.

1-2. SCOPE OF MANUAL

This instruction manual describes the MEC (Milgo Electronic Corporation) Model 75 Data Receiver, designed and manufactured by Milgo Electronic Corporation for International Business Machines, Federal Systems Division, Kingston, New York, in conjunction with Project Mercury.

1-3. PURPOSE OF MANUAL

1-3.1. This instruction manual is provided as an aid to better understanding the operation and theory behind the MEC Model 75 Data Receiver and its associated equipment. It offers a complete technical explanation coupled with applicable illustrations, with an estimation of the interest and questions of the qualified technician.

1-3.2. It is strongly urged that the operator, or any person involved in the operation of this equipment, thoroughly read and fully understand the contents of this manual.

CHAPTER II

GENERAL DESCRIPTION

2-1. GENERAL

The MEC Model 75 Data Receiver accepts four channels of data in serial form, aligns the data and shifts it out in serial form, in addition to internally generated copy pulses, to MEC Model 76 500 Bit Receiver. The Data Receiver contains two Model 165-4C Power Supplies, and should failure occur to the +12 volts or -20 volts of the primary supply, the respective voltage of the standby supply is automatically switched into operation. The Data Receiver also has facilities for testing most of its own circuitry.

2-2. PHYSICAL DESCRIPTION (Figure 2-1)

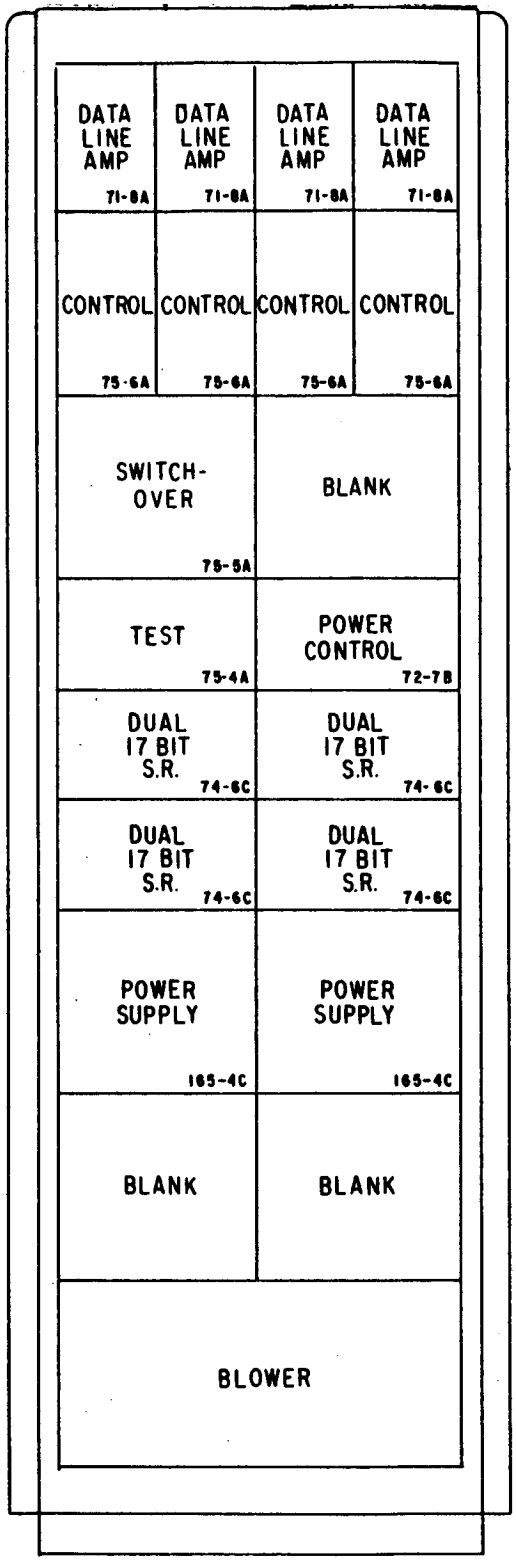
The Model 75 Data Receiver is housed in a standard rack approximately 74 - 1/8 inches high, 24 inches wide, and 22 inches deep. Its weight is approximately 500 pounds. All chassis are of modular construction and employ 50 pin connectors to effect the connection of each chassis to rack wiring. All Chassis of a particular type are interchangeable, and they are keyed making it impossible for insertion into an incorrect rack position. Rack Chassis are locked in place by a single screw type locking handle.

2-3. INPUTS

The Data Receiver accepts modulated tone bursts of approximately 2 kc, at a 1 kc repetition rate from voice channels on balanced or unbalanced 600 ohm communication lines, equalized for 1 kc data bit rate. Data may also be entered from a MEC Model 1585-1A Tape Recorder which contains pre-recorded data of the same form. Data consists of 0.5 millisecond bursts; EOW, a 4.5 millisecond burst. Input signal requirements are from -30 dbm to +10 dbm. Minimum signal to noise ratio is in the order of 3:1 in the band pass range. Outside this band pass range, attenuation should be at least 20 db per octave. The Data Receiver requires 120 vac single phase at approximately 8 amperes as power inputs.

2-4. OUTPUTS

2-4.1. An output exists from each of the four Data Line Amplifiers which provides modulated tone bursts that have been filtered and amplified for the purpose of recording the data on magnetic tape.



DATA RECEIVER
75-1A

FIGURE 2-1. CHASSIS ARRANGEMENT

2-4.2. In conjunction with each of the four receiver outputs, there is a pair of output circuits used for the output signal providing isolation on each of the lines to the Model 76 500 Bit Receiver. Therefore, there are 8 (4 pair) data outputs, 8 (4 pair) EOW outputs, and 8 (4 pair) copy outputs, for a total of 24 output lines. One output of a pair is designated A, the other is designated B. There are also provisions for signal ground reference.

2-4.3. Outputs levels are as follows:

A Binary "1" is 0 volts

A Binary "0" is -17 volts ±3 volts

2-4.4. From any Control Chassis, a 350 microsecond copy pulse should follow the presence of data on the data lines by less than 10 microseconds. Copy pulse should have the same relationship to EOW.

2-4.5. A form of visual checking in the Receiver is possible to the following extent. The data neon indicators will show an increased intensity for a pattern of all "1's" as compared to a pattern of alternate "1's". They will not light for a pattern of all "0's". The copy and EOW indicators should maintain the same intensity for all patterns.

CHAPTER III

THEORY OF OPERATION

3-1. GENERAL (Figure 9-1)

3-1.1. The Model 75 Data Receiver contains, in effect, four individual receivers capable of independent operation. Data on each channel enters a Data Line Amplifier, is detected, delayed within the system, if necessary, for alignment with other channels of data, and sent with an internally generated copy signal to the MEC Model 76 500 Bit Receiver. In the 500 Bit Receiver, three of the four channels are compared with each other and a composite data bit is obtained on a basis of at least two of the three channels being alike and correct.

3-1.2. The entire rack is powered by a single Model 165-4C Power supply, with an additional supply in standby, which, in the event of failure to either the -20 volts or +12 volts of the primary supply, the respective voltage of the standby supply will automatically be switched into operation. Facilities are also provided for measuring any of the internally generated voltages of the system, which includes the +250 volts and -250 volts, generated in each of the Data Line Amplifiers. Indicators are provided to indicate voltage failures in any of the Data Line Amplifiers.

3-1.3. The Receiver contains a Test Pattern Generator for simulating data from the Data Line Amplifiers for purposes of testing all four of the Control and Dual 17 Bit Shift Register Chassis. Four automatic test patterns may be generated: All "0's", a "1 - 0" pattern, a "0 - 1" pattern, and a pattern of all "1's".

3-1.4. Operate Mode - The Model 75 Data Receiver receives 4 channels of data from a source which is transmitting identical data on all four channels. These four channels may have various delays with respect to one another as determined at the transmitting site, with the limitation that the maximum delay is not greater than 16 milliseconds. (Delays are set in millisecond increments). The data arrives via 4 separate routes and will encounter additional delays of various amounts depending upon the routing and types of transmission equipment used enroute. Misalignment of the data at the source is done in order to lessen the possibility of external noise affecting all data lines in a like fashion once it leaves the source. It is convenient at this point to describe one of the four identical receivers within the receiver rack itself, consisting of a Data Line Amplifier, a Control Chassis, and a Dual 17 Bit Shift Register. (See Figure 9-1, Sheet 2 of 2).

3-1.4.1. Upon receiving information, the Data Line Amplifier separates the tone bursts into data pulses and EOW pulses.

NOTE

A pulse will occur on the data output of the Data Line Amplifier for an EOW tone burst, and is followed 4 milliseconds later by a pulse on the E OW output. This bit on the data output is not used as data.

The Data Line Amplifier also provides as an output, a clock signal in the form of a 1 kc sine wave which is synchronized to incoming data. Clock, Data, and EOW from the Data Line Amplifier enter the Control Chassis where they are delayed from 10 to 500 microseconds (referred to as vernier delay) to align them with respect to the remaining three channels. Data then enters a 4 bit shift register which compensates for the 4 millisecond time delay required to recognize EOW, in order that EOW, going into the 17 Bit Shift Register from the Control Chassis, follows the last bit of data by one millisecond. There may still be a time difference in millisecond increments, between data on the four channels.

3-1.4.2. The 17 Bit Shift Register is used to complete the alignment of the data and EOW on one channel with respect to another. The Shift Register shifts on pulses from the Control Chassis which are derived from delayed clock. The Shift Register provides from 0 to 16 milliseconds of delay in millisecond increments for both data and EOW, delaying both by the same amount. There are two outputs from each of the two Shift Registers, an A and B data output, and an A and B EOW output, and it is here where redundancy is started for the two outputs of each of the data and EOW signals to the 500 Bit Receiver. Each bit, from the outputs of the 17 Bit Shift Register, is stored for slightly less than one millisecond in the Control Chassis as they appear at the output lines, during which time copy pulses are generated. The output signals to the 500 Bit Receiver are composed of copy, data, and EOW. There are two outputs for each of the signals from each Control Unit. The characteristics of these outputs are discussed in more detail under paragraph 3-3.6.

3-1.5. Test Mode - The system is put in test mode by selecting one of the test patterns on the Test Pattern Generator. When in test mode, the TEST PLAYBACK indicator I401 is lit, providing an indication to the operator that the system is not in operate mode. Conversely, the test circuitry is inhibited when in the operate mode. To start generation of test patterns after leaving the operate mode, it is necessary to press the TEST START pushbutton S402. Test data is generated in sequences of approximately 500 milliseconds followed by EOW in a repetitive pattern.

3-1.5.1. When operating in test mode in conjunction with the 500 Bit Receiver, all Shift Registers should be set for identical delays. As data always is in serial form, the patterns can only be verified with an oscilloscope. However, the patterns are visible on the indicators of the 76 500 Bit Receiver.

3-1.6. Tape Recording Facilities - Incoming data to the Receiver may be recorded on a MEC Model 1585-1A Tape Recorder, if so desired. The data is recorded while the system is in operation and is furnishing data to the 500 Bit Receiver. The data is recorded in an identical form to that when it is received from the telephone voice lines, that is, in tone bursts, however, it is initially filtered and amplified prior to being supplied to the output connector. The Tape Recorder may be used for re-running the data at a later date for further analysis or test purposes.

3-1.6.1. Playback Mode - The Data Receiver is placed in the playback mode by positioning the four OPERATE-SIMULATE toggle switches, located in the rear of the rack, to the SIMULATE position. The TEST-PLAYBACK indicators I401 (located on the Test Pattern Generator Chassis), and I2 (located on connector mounting plate in the rear of the rack) will be on if any of the four switches are in the SIMULATE position. When all four switches are in the OPERATE position, the two indicators will be off. This mode is identical to the Operate mode (paragraph 3-1.4) with the exception of the source of data.

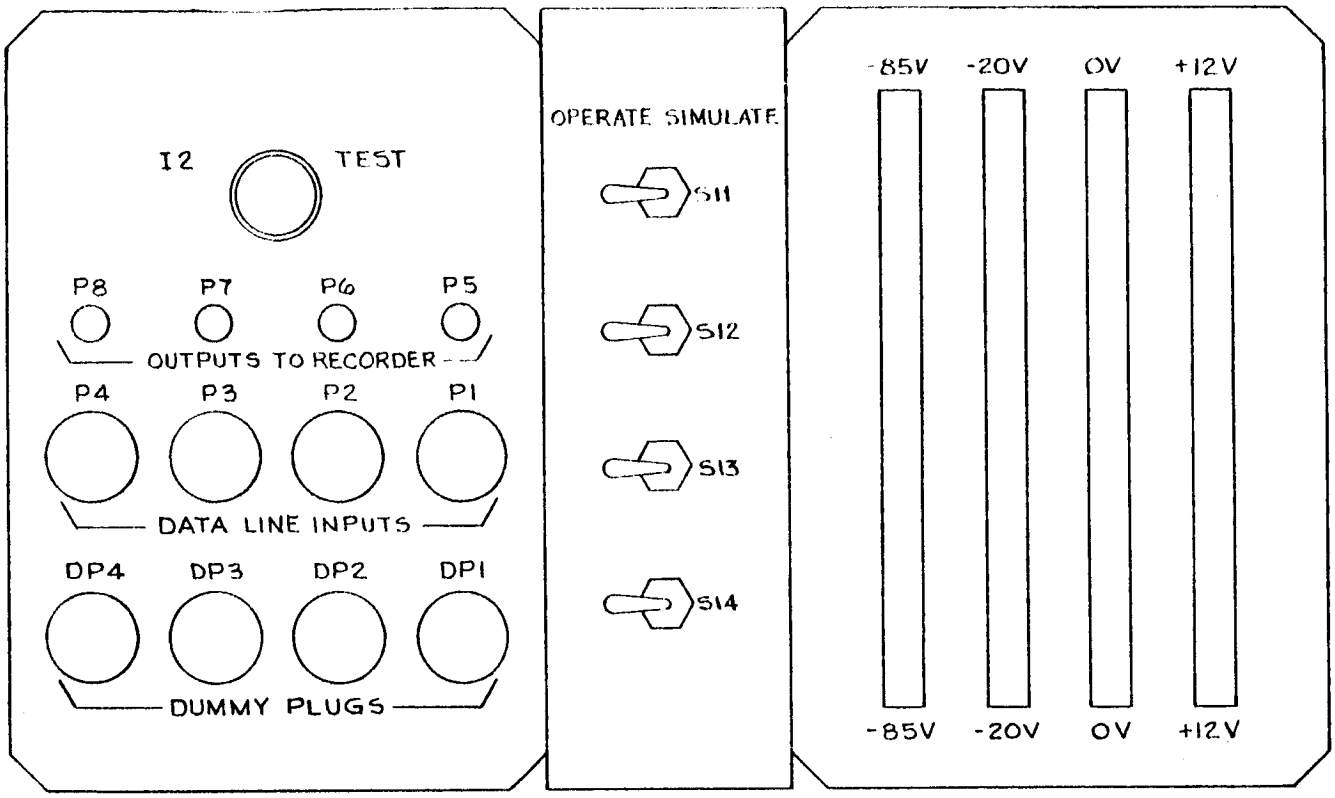


Figure 3-0. Operate-Simulate Switch Panel

3-2. DATA LINE AMPLIFIER, MEC MODEL 71-8A (See Appendix)

3-2.1. Data on all four channels entering the Model 75 Data Receiver initially enters the Data Line Amplifiers. The Data Line Amplifiers separate the incoming tone bursts into data pulses and EOW pulses, and also provides as an output a clock signal in the form of a 1 kc sine wave which is synchronized to the incoming data.

3-2.2. The Data Line Amplifier has facilities for accepting a SOW burst, however, SOW is not required in this system. EOW burst is a 4.5 millisecond burst at 2 kc. Data "1" is comprised of 1 cycle at 2 kc.

3-2.2. A detailed description of the Model 71-8A Data Line Amplifier may be found in the Appendix of this manual.

3-3. CONTROL CHASSIS, MEC Model 75-6A (Figures 3-1, 9-4, and 9-5)

3-3.1. The Control Chassis receives data, EOW, and clock from the Data Line Amplifier, provides delays for vernier alignment of these inputs and generates shift pulses. Data and EOW are then delayed for major increment alignment in the Dual 17 Bit Shift Register. The Control Chassis also accepts data and EOW from the 17 Bit Shift Register and provides them as outputs to the 500 Bit Receiver, with copy pulses which are generated in the Control Chassis.

3-3.2. In the Operate mode, data, in the form of positive pulses from Data Line Amplifier, enters the Control Chassis at pin 1 of P601. Diode CR601 is back biased with respect to positive pulses with -20 volts at its plate. Data pulses trigger variable one-shot N616 at pin 3. (The procedure for adjusting this and other variable one-shots in the Control Chassis is described under CHAPTER IV, OPERATION). The output of one-shot N616, pin 5, after the desired delay, becomes positive and triggers a 20 microsecond one-shot, N601, which produces a positive pulse for inserting data into core M601. Resistor R603 is a series limiting resistor limiting the core setting current to approximately 10 ma. Data is shifted through cores M601 through M604 and out of the Control Chassis via pin 12 of P601 to the Dual 17 Bit Shift Register Chassis. The shift pulses to the cores, both in the Control Chassis and the Dual 17 Bit Shift Register Chassis, are generated from the 1 kc from the Data Line Amplifier which enters the Control Chassis on pin 3 of P601. Diode CR603 is back biased

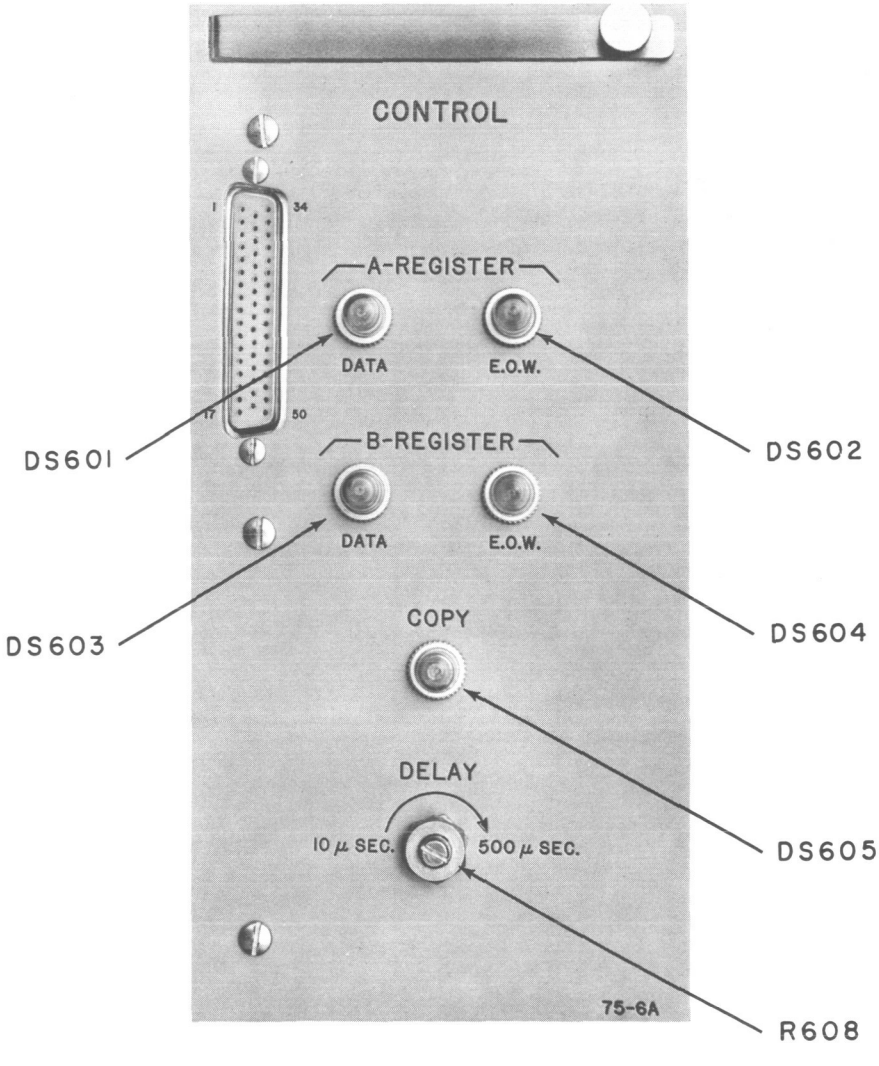


Figure 3-1. Control Chassis

in the operate mode with approximately -10 volts on its plate. The incoming 1 kc, in the form of a sine wave, enters pin 3 of Schmitt Trigger N602. The Schmitt Trigger output at pin 5 approximates a square wave which is out of phase with the input. Variable one-shot N603 triggers on the positive going output from the Schmitt Trigger. Referring to Figure 3-2 the relationship between data and clock can be seen. Variable one-shot N603 has been set to align its positive going trailing edge with the three remaining receivers. This action determines the setting of one-shot N616, which is adjusted to produce data insertion into core M601 approximately 500 microseconds following delayed clock which produces a shift pulse, or, more specifically, half-way between shift pulses. The output of N603, at pin 5, on its positive going edge, triggers the 10 microsecond one-shot N604. N604 goes positive at its output, pin 7, when triggered. This pulse is used to reset the flip-flops receiving data from the 17 Bit Shift Register. The positive going trailing edge of the pin 5 output of N604, is a-c coupled to emitter follower N605 through capacitor C610 and resistor R612. Diode CR604 is used for fast discharge of C610 on a negative going pulse so that 10 microseconds later, when the incoming pulse goes positive, there will be a full amplitude pulse at the output of the emitter follower N605 (pin 3). This emitter follower drives three core drivers, N606 in the Control Chassis, and N601 and N604 in the Dual 17 Bit Shift Register Chassis. Core driver N606 in the Control Chassis is used to shift cores M601 through M604. The four cores, when shifted at 1 kc, provide 4 milliseconds of delay for incoming data. Since it takes 4 milliseconds to recognize an EOW code burst, EOW from Data Line Amplifier will occur 5 milliseconds after the last data bit of a message. (EOW code burst starts one millisecond after the last data bit.) With the 4 milliseconds of delay just mentioned, the last bit of data will enter the Dual 17 Bit Shift Register one millisecond before EOW. To state it another way, EOW will enter the register coincident with a dummy one bit that occurs on the data line from Data Line Amplifier at the beginning of an EOW code burst.

3-3.3. EOW from the Data Line Amplifier enters the Control Chassis at pin 2 of P601. R610 and R609 provide cathode resistors to -20 volts for the EOW cathode follower in the Data Line Amplifier. EOW pulses trigger variable one-shot N617 at pin 3. Resistor R650 is adjusted to provide a positive going trailing edge approximately between shift pulses derived from delayed 1 kc. The output at pin 5 of N617 triggers one-shot N618, a 20 microsecond one-shot, which inserts EOW into core M602 in the Dual 17 Bit Shift Register Chassis. R651 is a series limiting resistor limiting the core setting current to approximately 10 ma. (See Figure 9-3 for waveforms of data and EOW to 17 Bit Shift Register.)

3-3.4. At this point it has been shown how data and EOW arrive at the Dual 17 Bit Shift Register and how shift pulses are generated. The remaining circuitry in the Control Chassis deals with the data after it leaves the Shift Register, having been delayed an integral number of milliseconds.

3-3.5. Data returns to the Control Chassis via two separate lines from the Shift Register. Both lines contain identical information in each case and are identified as A and B. The A and B data lines enter the Control Chassis on pins 8 and 4 of P601, respectively. The A data sets flip-flop N607 at pin 3; the B data sets flip-flop N609 at pin 3. The outputs, at pin 8, of these flip-flops drive emitter followers which serve as outputs of the system to the 500 Bit Receiver. (See Figure 9-3 for data waveforms to B shift register.) Data leaving the 17 Bit Shift Register occurs shortly (approximately 6 microseconds) after the shift pulse is initiated.

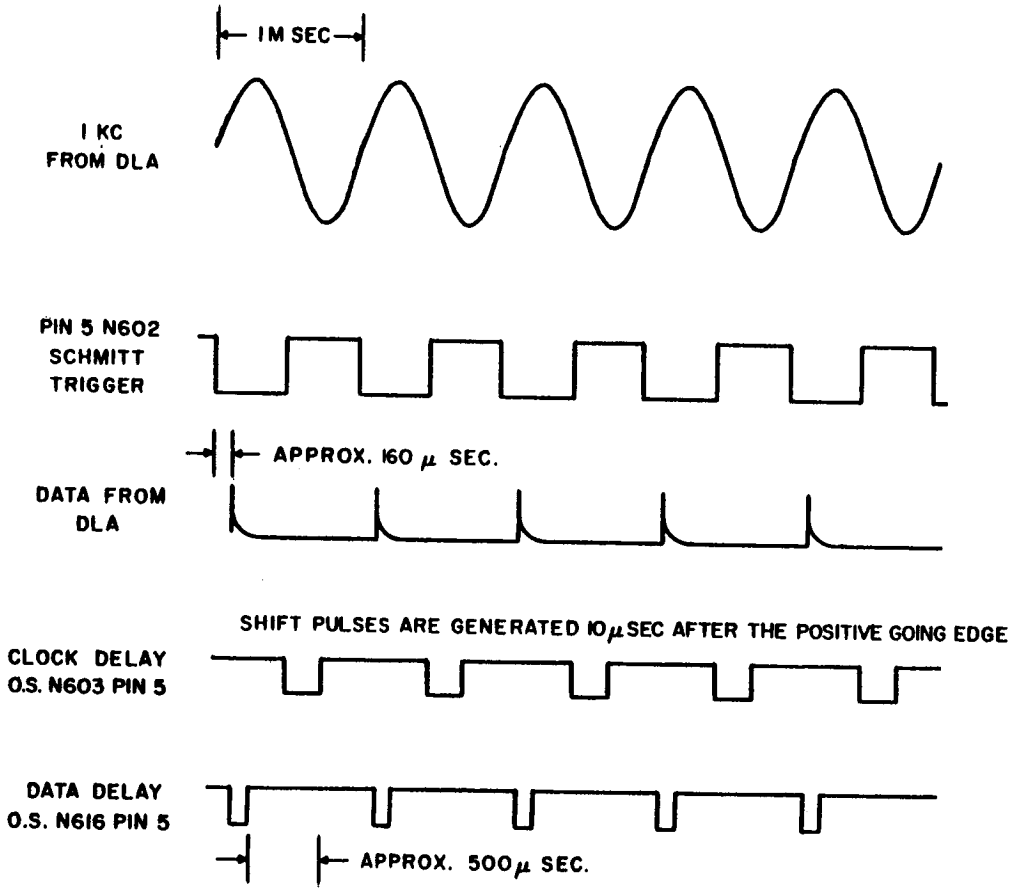


Figure 3-2. Voltage Waveforms

3-3.6. Flip-flops N607 through N610 in the Control Chassis are reset 10 microseconds before a shift pulse is generated with the leading edge of one-shot N604. Therefore, the flip-flops will be reset less than 20 microseconds before they receive new data. Flip-flops N608 and N610 receive EOW A and EOW B in a manner identical to the data flip-flops just mentioned. The EOW flip-flops also have emitter followers from their outputs at pin 8 for the purpose of providing EOW outputs to the 500 Bit Receiver. (See Figure 9-3 for EOW waveform to B Shift Register.)

3-3.7. A copy pulse is sent with data to the 500 Bit Receiver to indicate when new data is appearing. The copy pulse must not occur until after the data lines have received new data. The positive going trailing edge of one-shot N604 at pin 5, which initiates a shift pulse, also triggers one-shot N611. N611 generates a copy pulse on its positive going trailing edge after 10 microseconds by triggering one-shot N612 at pin 3, which is a 200 microsecond one-shot. The output of N612 at pin 7 drives two emitter followers which provide isolation on the two copy lines to the 500 Bit Receiver, which are the outputs of the two emitter followers. (See Figure 9-3 for copy waveform to A Shift Register.)

3-3.8. In test mode the Control Chassis functions in an identical manner to that previously discussed, with the exception that artificially generated data and EOW are used to replace outputs from the Data Line Amplifier. The 1 kc oscillator in the Data Line Amplifier operates continually, even during data absence, producing an output from which test data may be derived. Since there is no synchronization between the four Data Line Amplifiers, one of the Data Line Amplifier clocks is used for generating test data for all four receivers. Data Line Amplifier 1 is arbitrarily selected to provide 1 kc for generating test data. When the Test Pattern Generator is set for one of the test patterns, -20 volts is removed from pin 40 of P601 on Control Chassis, 2, 3, and 4. This puts +12 volts through resistor R604 and diode CR603 at the input of Schmitt Trigger N602 in these three chassis. Control Chassis 1, however, has pin 40 jumpered to -20 volts and does not affect the Schmitt Trigger during test mode. It continues to operate on 1 kc from Data Line Amplifier 1. The output of Schmitt Trigger N602, pin 5, in Control Chassis 1, is connected through resistor R607 to pin 41, which is the input to the Test Pattern Generator for deriving data and 1 kc pulses. The generated 1 kc pulses in the Test Pattern Generator enter Control Chassis 2, 3, and 4, on pin 41. In this way the one-shot N603 in all four Control Chassis are operating, for all practical purposes, in unison.

3-3.9. When generating test patterns, -20 volts is removed from the test data line, pin 38 in the Control Chassis, and positive pulses representing test data appear at pin 38. (See Figure 9-3 for Test Data waveform.) In a similar fashion, on pin 39, during test pattern generation, -20 volts is removed and test EOW pulses occur at pin 39. (See Figure 9-3 for Test EOW waveform.)

3-4. DUAL 17 BIT SHIFT REGISTER, MEC MODEL 74-6C (Figures 3-3, 9-6 and 9-7)

3-4.1. The Dual 17 Bit Shift Register delays data and EOW on any channel, if necessary, for purposes of aligning the channel with respect to the remaining channels. This action compensates for delays between channels initiated at their source, and delays encountered en route to the Receiver. The chassis provides delays of up to 16 milliseconds, in millisecond increments, for both data and EOW.

3-4.2. N601 and N604 are core drivers used to shift the cores in the chassis. A trigger pulse is required on pin 1 of P601 to trigger both core drivers. Data is delayed in M619 through M635, while EOW is delayed in M602 through M618.

3-4.3. Data "1's" are inserted in the input winding, pin 8, of the first core M619 on the data delay cores. EOW "1's" are inserted on the input winding, pin 8, of the first core, M602, in the EOW delay cores. The output of each core travels to two switches in addition to the next core.

3-4.4. Each switch is a two pole, 16 position, rotary switch, with data on one set of stationary contacts and EOW on the other set of stationary contacts. Each contact on the data pole of the switch corresponds time-wise to the contacts on the EOW pole. For example: Pin 4 on the data side originates from the output of the 4th data core, and pin 4 on the EOW side from the output of the 4th EOW core. This means that if pulses are inserted in both EOW and data cores at the same time, they will both appear at the proper No. 4 pin, four time slots (four milliseconds) later. The rotary contact of each pole is connected to the inputs of separate flip-flops in the Control Chassis, and each will arrive delayed by four time slots.

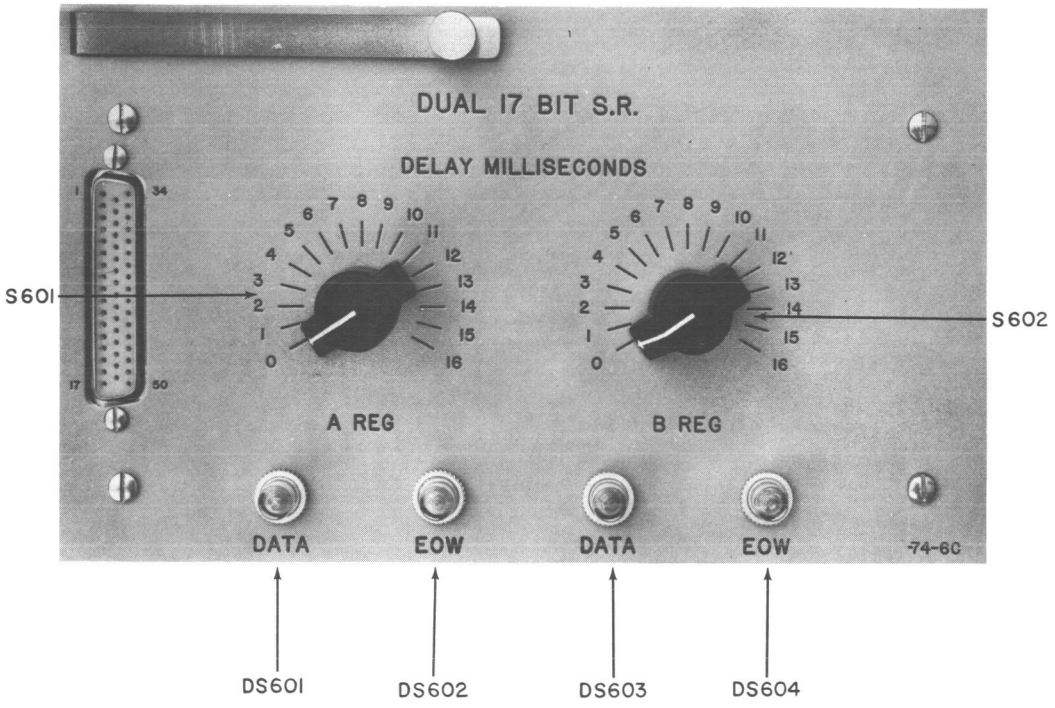


Figure 3-3. Dual 17 Bit Shift Register

3-4.5. The output of each core is connected to two double pole, 16 position switches, wired as described above. In this fashion, the two outputs for data and EOW, required for each input, are obtained. Both switches must, therefore, be set for identical settings for proper operation. The rotary contacts are also connected to one-shots in the 17 Bit Shift Register Chassis. Both EOW contacts are connected to 100 millisecond one-shots, while the data rotary contacts are connected to 200 millisecond one-shots. These one-shots drive neon indicators located on the front panel of the chassis, providing visual indication of data and EOW being sent to the Control Chassis. Each time a pulse is sent to the Control Chassis, the indicator will light; the data indicators staying on for 200 milliseconds and the EOW indicators staying on for 100 milliseconds.

3-4.6. The positions of the delay switches on the front panel are numbered 0 through 16. These figures represent the amount of time delay. Since the cores are shifted every millisecond, the switches indicate delay in milliseconds.

3-5. TEST PATTERN GENERATOR, MEC MODEL 75-4A (Figures 3-4, 9-8 and 9-9)

3-5.1. The Test Pattern Generator generates four selectable patterns of artificial data bits in the form of approximately 500 millisecond bursts, followed by an artificially generated EOW pulse. Switch S401, on the front panel, is used to select operate mode or one of the four test patterns.

3-5.2 N401A and B are cross-coupled amplifiers which make up a 500 millisecond free-running multivibrator (FRMV). The TEST START pushbutton S402, applies +12 volts through resistor R410 to pin 2 of N401A. If S401 is in the OPERATE position, a positive voltage is applied through S401A, CR401A, CR404, and R407 keeping pin 2 of N401A positive and preventing N401 from functioning as a multivibrator. When S401 is placed in any of the test pattern positions, pin 2 of N401 is biased negatively through R409. When the TEST-START pushbutton is pressed, the +12 volts to pin 2 of N401 initiates the multivibrator action.

3-5.3. One-shot N402 receives 1 kc from the Schmitt Trigger, N603, in Control Chassis #1. It generates 100 microsecond pulses at a 1 kc range. The one-shot is kept off during operate mode by applying approximately +12 volts to pin 6 through diode CR412 from switch S401A in a similar fashion to that just described for N401. The output of N402 at pin 7 provides 1 kc to Control Chassis 2, 3, and 4 during test mode, and is also the output used for generating a data pattern of all"1's" through position 5 of S401B. The output of N402 at pin 5 drives the count input of flip-flop N403. The two outputs of N403 provide the alternating data patterns.

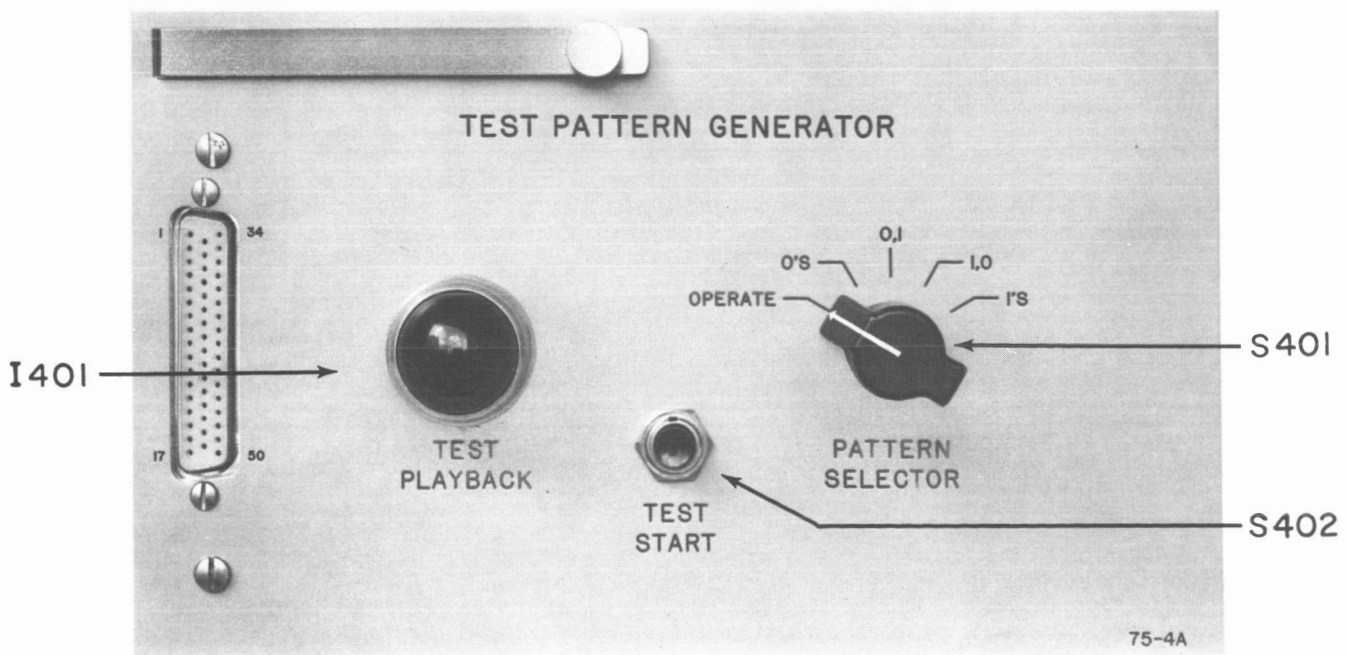


Figure 3-4. Test Pattern Generator

The pin 5 output is used for a data pattern "0-1" to position 3 of S401B. The pin 8 output in a like fashion, provides a "1-0" data pattern to position 4. In addition, this output is used to synchronize EOW with data, as described in the following paragraph.

3-5.4. When pin 4 of N401A is at -20 volts, the junction of resistors R406 and R403 is approximately -20 volts. With diode CR407 biased in this fashion, a pulse from pin 8 of flip-flop N403 cannot trigger flip-flop N404. When pin 4 of N401A rises to 0 volts, the junction of R403 and R406 is approximately -2 volts. The next occurring positive pulse from pin 8 of flip-flop N403 triggers flip-flop N404 at pin 3. Pin 8 of N404 goes positive at this time, generating a pulse to emitter follower N405A which produces a test EOW pulse to the four Control Chassis. Approximately 250 milliseconds later, pin 5 of N401B goes to 0 volts. With a gating circuit identical to that just discussed, the next positive going pulse at pin 8 of N403 triggers flip-flop N404 at pin 6, causing the output at pin 8 to return to -20 volts, thereby preparing the flip-flop for a repetitive cycle. For clarity, the functions of each deck of switch S401 will be described.

3-5.4.1. S401A has approximately +12 volts on the wiper in the OPERATE position (position 1). This biases off the FRMV N401 and the one-shot N402. In addition, S401A energizes relay K401 which controls the voltage to the TEST-PLAYBACK indicator, I401. The lamp has 110 vac applied to it when the relay is de-energized. In positions 2, 3, 4, and 5, S401A has -20 volts on the wiper, the bias is removed, and the relay has 0 volts across the coil. In order for the relay to be energized, the 4 input connectors must be in place, as they provide, as an interlock function, -20 volts to one side of the relay coil.

3-5.4.2. The wiper of S401B is the data output to the Control Chassis in the test pattern positions. In position 1, -20 volts is applied to the wiper, which back biases diodes in the Test-Data output lines. Position 2 applies +12 volts to the wiper for all "0's". Positions 3 and 4 receive alternate data patterns from flip-flop N403. Position 5 receives all "1"s from one-shot N402.

3-5.4.3. S401C applies -20 volts to the test gate inputs of Control Chassis 2, 3, and 4, when in the OPERATE position. This back biases CR603 in the Control Chassis, allowing the Schmitt Trigger to operate normally on clock from the Data Line Amplifier. In positions 2, 3, 4, and 5, this connection is open, and diode CR603 biases off the Schmitt Trigger from +12 volts. This switch is connected only to Control Chassis 2, 3, and 4, as the Schmitt Trigger in Control Chassis 1 functions normally in test modes.

3-6. SWITCHOVER CHASSIS, MEC MODEL 75-5A (Figures 3-5, 9-10, and 9-11)

3-6.1. The Switchover Chassis monitors the +12 volt and -20 volt outputs of the primary Power Supply and automatically switches either voltage from the secondary supply to the system if the primary voltage deviates from its limits. (The -85 volts is switched with the -20 volts.)

3-6.2. The A supply (right hand supply) is the primary supply. As long as meter relay MV501 is within limits, voltage is not applied to terminal C or E. The voltage divider consisting of resistors R504 and R509 provides a positive voltage to pin 2 of pulse amplifier N501A, causing the transistor to be turned off. The output, pin 4, is at -20 volts in this case, and there is no drop across relay K501. With K501 de-energized, relay K504 has an open connection to its coil, (pins 4 and 5 of K501), and +12 volts from the A supply, (pins 4 and 5 of P501) is connected to pins 43 and 44 which supply +12 volts to the 12 volt bus. Should +12 volts from the A supply go off limits as set on MV501, contact is made between D and E or D and C of MV501. This applies -20 volts through the meter relay contacts to R503, producing a negative voltage at pin 2 of pulse amplifier N501A, thereby turning on the transistor. The output, pin 4, then goes to 0 volts, energizing K501 which in turn supplies -20 volts through contacts 4 and 5 to relay K504. When K504 is energized, +12 volts from the B supply is connected to the 12 volt bus through contacts 2 and 3 of K504. Energizing K501 also supplies power through contacts 2 and 3 to I504, indicating that +12 volts is off limits. When K504 is energized, power is supplied through contacts 4 and 5 to I502 indicating +12 volt switchover. The switchover may be returned to the original state with pushbutton S501,

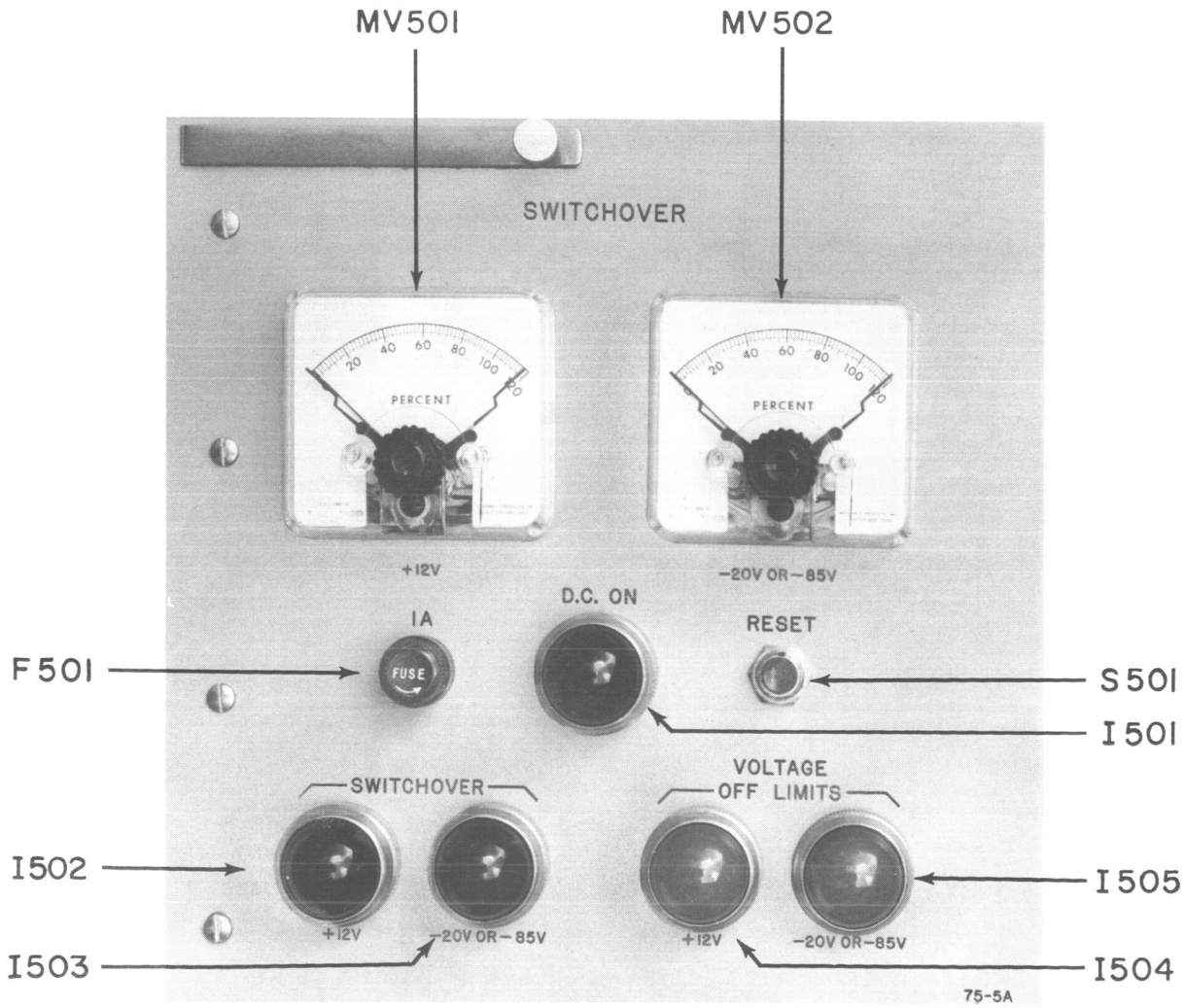


Figure 3-5. Switchover Chassis

which interrupts the emitter return to 0 volts of N501A through terminals 1 and 2 of the pushbutton, and by so doing, removes current from K501. This, in turn removes -20 volts from pin 8 of K504, and returns the A Supply to the connection to the +12 volt bus.

3-6.3. When -20 volts is within limits, meter relay MV502 does not make contact between D and C or D and E. The -20 volts is connected to pin 7 of N501B through resistors R506, R507, and R508. This biases the transistor in pulse amplifier N501B into saturation, energizing relay K507. When K507 is energized, the -20 volt indicator, I505 is extinguished by the opening of contacts 1 and 2, and contacts 5 and 6 are open, leaving no current path through the coil of K503. When K503 is de-energized, contacts 1 and 2 supply -20 volts to relays K505 and K506 which connect -20 volts from the A supply to the -20 volt bus. (Relay K506 also connects -85 volts from the A supply to the -85 volt bus.) When -20 volts is applied to the -20 volt bus, relay K502 is energized, shorting out series limiting resistor R512. When -20 volts from the A supply goes off limits, meter relay MV502 applies +12 volts to terminal D, biasing pin 7 of pulse amplifier N501B positive, turning N501B off, and removing current from relay K507. When relay K507 is de-energized, I505 indicates that -20 volts is off limits. Contacts 5 and 6 of K507, which provide a current path to 0 volts from -20 volts for relay K503, are closed, energizing K503. When K503 is energized, contacts 1 and 2 open, removing power from relays K505 and K506, which disconnects the -20 volts and -85 volts from the A supply, and connects the B supply to the wires of the respective busses. Relay K503, when energized, also supplies power to I503, indicating switchover of the -20 volts and -85 volts. When -20 volts to the bus momentarily drops, relay K502 is de-energized, opening the contacts across series limiting resistor R512 and closing the contacts across limiting resistor R511. As power is returned to the bus, K502 is again energized, this time from the B supply, and R512 is again shorted through the relay contacts. Relay K508 is connected between the outputs to the +12 volt bus and the -20 volt bus, and is energized as long as both voltages are present at the busses. This relay controls power to I501 which indicates when d-c power is on.

3-6.4. Resetting to the A supply is accomplished with pushbutton S501. The circuit operation when resetting +12 volts has already been discussed. When the pushbutton is pressed for -20 volts and -85 volts, +12 volts is removed from meter relay MV502, allowing pulse amplifier N501B to return to its saturated state, which causes all relays in the -20 volt switchover circuitry to return to their initial conditions.

3-7. POWER CONTROL CHASSIS, MEC MODEL 72-7B (Figures 3-6, 9-12 and 9-13)

3-7.1. The Power Control Chassis provides the means for switching a-c power to the rack, measurement of all internally generated voltages, and has indicators to provide visual detection of power failures in the Data Line Amplifiers.

3-7.2. AC power is switched to the system via switch S701. When power is on, neon DS701 is on. Diode CR701 rectifies the a-c for measurement. Meter MV701 and switch S702 are used to measure 120vac, the 3 d-c voltages from both A and B supplies (+12 volts, -20 volts, and -85 volts) and the +250 volts and -250 volts generated within each of the four Data Line Amplifiers. MV701 is a 1.2 ma. meter. By limiting the current from each voltage to 1 ma. with an appropriate 1% resistor, all voltages read approximately "10" on the meter, representing 100%, when properly adjusted. For optimum usage of the meter, however, the procedure in the following paragraph is recommended.

3-7.3 Using an external meter such as a Simpson Model 270 or Triplett Model 630, correctly set each of the 3 d-c voltages of both supplies while under load. This is discussed under CHAPTER IV, OPERATION. The voltages are brought out to the front of the power supply and clearly identified via test jacks TJ401 through TJ404. Record the reading of panel meter MV701 for all voltages on the VOLTAGE SELECTOR switch. The recorded readings may now be used to determine any discrepancy of system voltages. In general, the +12 volts, -20 volts, and -85 volts will read "10" ± 3%. The +250 volts will read "9.5" ± 5%; the -250 volts will read "10" ± 5%.

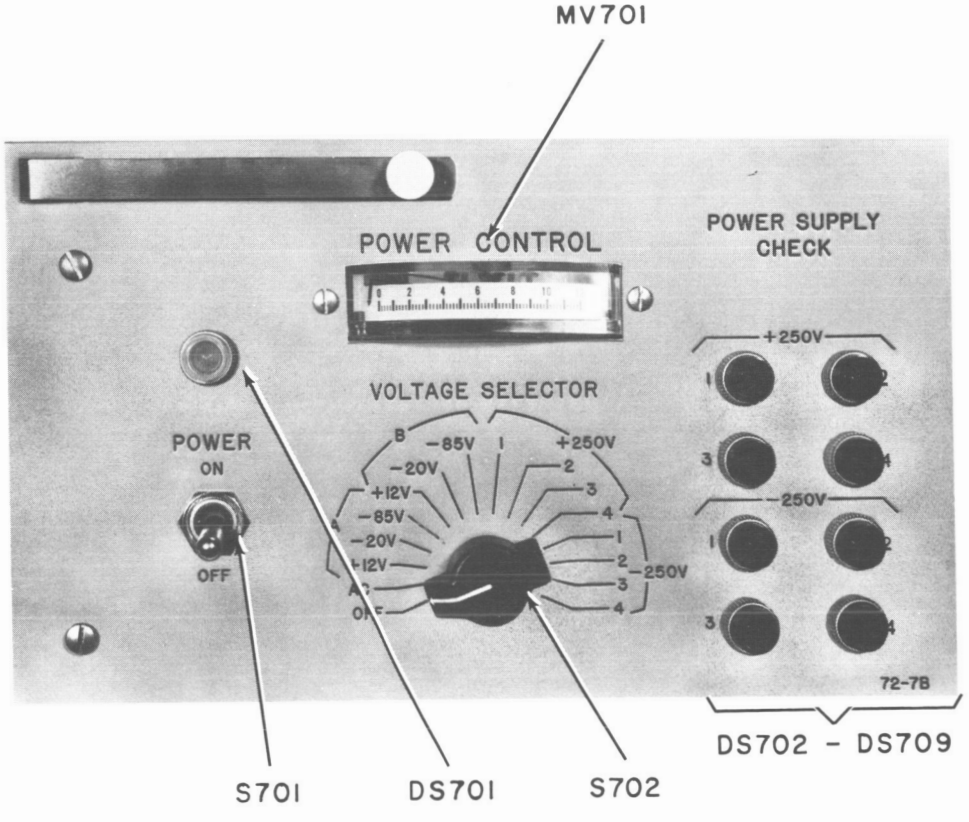


Figure 3-6. Power Control Chassis

3-7.4. There are eight neon indicators for monitoring the +250 volts and -250 volts from the Data Line Amplifiers. One group will be described. The four +250 volt lines are "or" gated through diodes CR702, CR703, CR704, and CR705. The common point of these diodes provides power to all four of the indicators, DS702, DS703, DS704, and DS705 through 100K limiting resistors. As long as power failure does not occur, each indicator has +250 volts applied to both sides and remains off. Should one supply fail, one side of the neon loses +250 volts and lights. A ground path is provided, using 100K resistors to ground in case the Power Supply failure is an open.

CHAPTER IV

OPERATION

4-1. General - When all connectors are properly connected and a-c power is supplied to the Receiver, place a-c power switch S1, located at the rear of the rack, to the ON position. A red indicator I1, adjacent to the switch, indicates when power is on (see Figure 4-1). This switch controls the 120vac to the Power Control Chassis, MEC Model 72-7B. Switch on a-c power to the system via switch S701, located on the front panel of the Power Control Chassis. A neon indicator DS701 located above the switch indicates when power is on. Power indicators on each of the Data Line Amplifiers will be lit at this time. The power supply check indicators on the Power Control Chassis should not be lit. The DC ON lamp on the Switchover Chassis will be lit, as well as SWITCHOVER and VOLTAGE OFF LIMITS indicators.

4-2. General Checkout Procedure - Set the VOLTAGE SELECTOR switch S701 to AC. The meter, MV701, should read "10" ±10%. Check and set the B Power Supply voltages using a Triplett 630NA VOM or equivalent. (The designation A refers to the left hand supply; B the right hand supply.) Press RESET pushbutton S501 on the Switchover Chassis. The SWITCHOVER and VOLTAGE OFF LIMITS indicators will now go out. Check and set A Power Supply voltages. Once these voltages have been set, the readings will not vary more than ±3%. The +250 volt readings should indicate 9.5 ±3%.

4-2.1. In checking Switchover operation, remove the a-c fuse from the A supply. The meter relay pointers will drop indicating Power Supply failure, and SWITCHOVER and VOLTAGE OFF LIMITS indicators will light. When the fuse is replaced and the RESET pushbutton pressed, the meter relays will return to a normal reading and the two indicators will go out.

4-2.2. In checking power supply check indicators located on the Power Control Chassis (for voltages generated in the Data Line Amplifiers), remove the a-c fuse from one Data Line Amplifier. The corresponding indicators for +250 volts and -250 volts will light. (The units are numbered 1 through 4 from left to right.) Turn power switch S701 on the Power Control Chassis off before replacing the fuse. The RESET pushbutton should be pressed each time power is restored. At least one of the Data Line Amplifiers must have power on in order for the indicators to operate, as power for the indicators is supplied by any or all of the functioning Data Line Amplifiers.

4-2.3. Set the PATTERN SELECTOR switch on the Test Pattern Generator to the ONE'S position and press the TEST START pushbutton S402. The TEST PLAYBACK indicator will be lit. (For the following checks the Data Line Amplifier inputs, P1 through P4, at the rear of the rack should be removed.) Set all four core drivers (shift) for minimum delay by turning potentiometer R608, located on the front panel of the Control Chassis, counter-clockwise as indicated on the front panel. For the following adjustments a Tektronix Oscilloscope Type 545A with CA plug-in, or equivalent, is required. The following described test jack locations are in the Control Chassis. Using test EOW as synchronization (TJ601-39), compare EOW insert (TJ601-35) on A trace with core drive (TJ601-5 or 6 in 17 Bit Shift

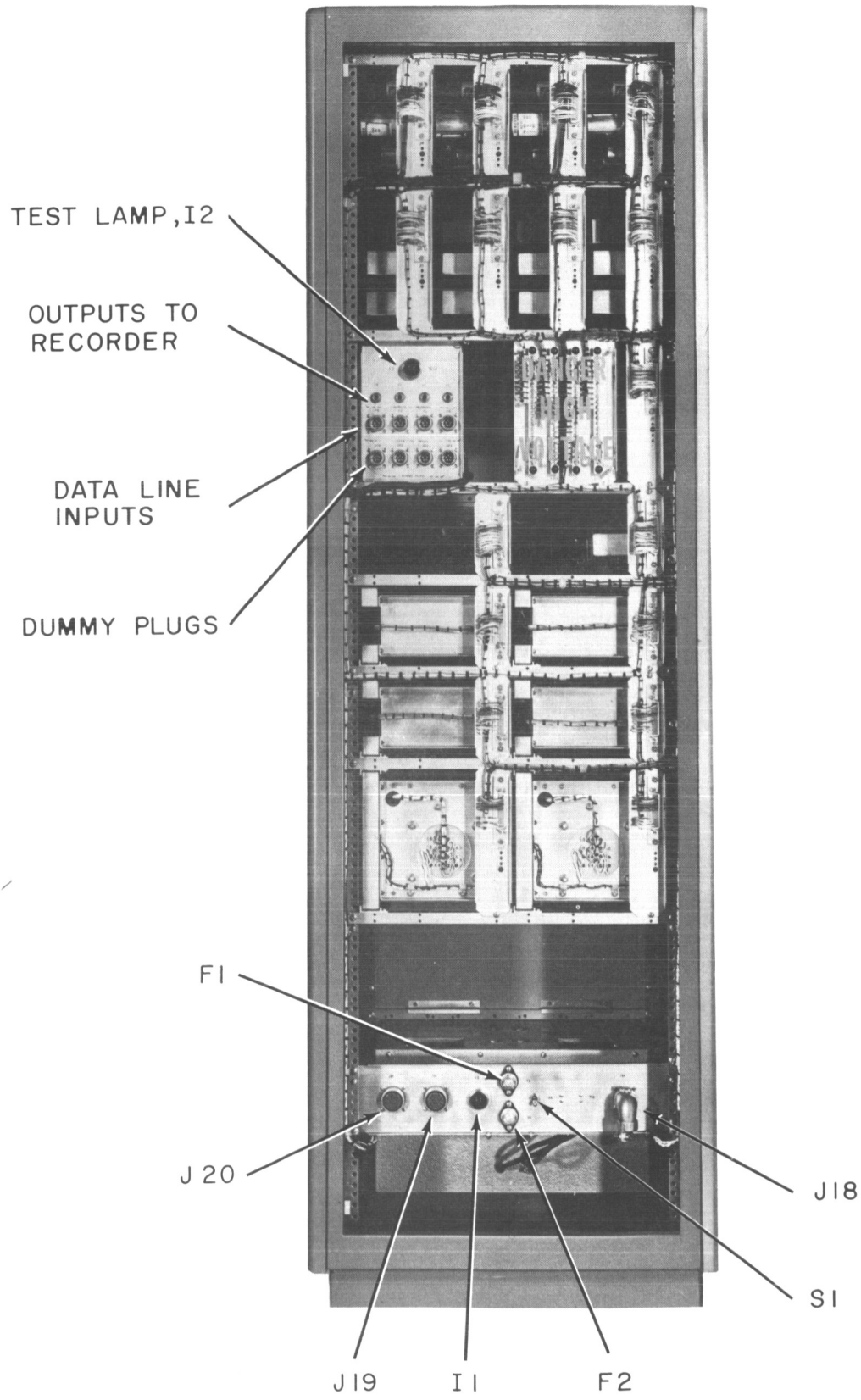


Figure 4-1. MEC Model 75 Data Receiver, Rear View

Register Chassis) on B trace. Adjust EOW delay potentiometer R650 until EOW insert is interlaced between two core drives. (It is necessary to remove the chassis and use an extension cable for this and the following adjustment.) Using the same synchronization, compare data insert (pin 7 of N601) with core drive (T-J 601-5 of the 17 Bit Shift Register). Adjust data delay, R648, until the data insert one-shot is interlaced between core drives. Repeat both of the above adjustments for all four Control Chassis. At this point, all data and copy indicators will glow. EOW indicators will flash at approximately 2 cycles per second.

4-2.4. Set all Shift Register Chassis for a maximum delay of 16 milliseconds. This provides checking for the maximum possible amount of circuitry.

4-2.5. The next check to be described is at the data outputs to the Model 76 500 Bit Receiver. A binary "1" is 0 volts; a binary "0" is -20 volts. As the data flip-flops are reset approximately 10 microseconds before each core drive, with a data pattern of all "1's", the A and B data outputs (TJ601-16 and 34) should be at 0 volts continually, with approximately -20 volt pulses, 10 microseconds wide, occurring at 1 millisecond intervals. Check all four Control Chassis.

4-2.6. The A and B copy pulse outputs (TJ601-13 and 14) are 200 microsecond positive pulses (binary "1") occurring at 1 kc. Check all four control chassis. The A and B EOW outputs (TJ601-13 and 14) are positive pulses approximately 1 millisecond wide, occurring approximately every 500 milliseconds. Check all four Control Chassis.

4-2.7. Switch the PATTERN SELECTOR switch S401 to a "1-0" pattern. Copy and EOWindicators should appear the same as for a data pattern of all 500 Bit Receiver "1's". Data indicators will decrease in intensity. When operating in conjunction with the 500 Bit Receiver, the test pattern will be visible on its indicators. Changing to a "0-1" pattern will provide the same indications as a "1-0" pattern in the Data Receiver, however, the pattern will change in the 500 Bit Receiver.

4-2.8. Select the 0's pattern. All data indicators will be extinguished, however, EOW and copy indicators will not change in appearance.

4-2.9. The preceding exercise checks the system to ascertain that it is functioning properly. It is not necessary to perform all the steps each time the system is operated. For example, voltages may be checked periodically, but do not necessarily require re-adjustment each time the system is turned on, once they have been set. This completes the test portion of system operation.

4-3. Operate - Connect the data input lines at the rear of the rack. Set all shift registers for a 0 millisecond delay. Switch the PATTERN SELECTOR switch to OPERATE. Adjust all four Data Line Amplifiers as described under paragraph 2-8 in DATA LINE AMPLIFIER, APPENDIX. It is necessary to have a test pattern transmitted from the Model 74 Data Transmitter to provide incoming data to the Data Line Amplifiers.

4-3.1. Examine all four EOW outputs from the Shift Register Chassis (TJ601-8 or 9) and determine their relative positions. (The four Shift Register Chassis are numbered 1, 2, 3, and 4 from left to right, top pair first.) This is most easily accomplished with a trial and error procedure of using one of the four for synchronization and observing the remaining EOW pulses until the first incoming EOW pulse is found. This may then be used for synchronization and the relative positions of the remaining EOW pulses may be determined. It is desirable to first set the millisecond increment delay so delays of less than one-half millisecond are more readily determined. The following examples describe how this is accomplished.

4-3.2. Figure 9-2(A) illustrates four possible EOW outputs as seen at the output of the 17 Bit Shift Register Chassis. These pulses are not necessarily delayed in any order, nor are they separated by exact millisecond increments. The adjustment being described is to align these pulses to the nearest half millisecond. To accomplish this it can be seen that #1 must be delayed 4 milliseconds; #2, 9 milliseconds; #3, 0 milliseconds (#3 already has the largest delay of all 4 lines), and #4, 10 milliseconds. (Both switches on each 17 Bit Shift Register are set for the same delay.) Figure 9-2(B) illustrates how the EOW pulses appear after the appropriate delays have been set. The pulses now all occur within 500 microseconds. It is now possible to determine which lines must be adjusted to accomplish vernier delay. In the example, as the #1 line already has the greatest remaining delay, lines #2, #3, and #4 should be delayed to line up with #1. Synchronize on #1 EOW, TJ601 pin 8 or 9 of Shift Register Chassis 1, and observe core drive of #1 (TJ601-6 in the Shift Register Chassis) and core drive of #2. Adjust potentiometer R608 on the front panel of Control Chassis 2 until the two are aligned. If jitter exists on the two lines, the delay adjustment should be determined on a basis of minimum excursion from #1, rather than an adjustment making the two occur simultaneously most of the time. Repeat the delay adjustment on Control Chassis 3 and 4 aligning them with #1. If Control Chassis 1 was properly set for testing, it is not necessary to make further adjustments on it. However, Control Chassis 2, 3, and 4 must have data and EOW delay adjustments reset in order to insert data and EOW mid-way between core drives. This adjustment is described under paragraph 3-3.5. Referring to EOW outputs from the 17 Bit Shift Register, these pulses should now be aligned and excursion due to jitter should not exceed ±125 microseconds.

CHAPTER V

INSTALLATION

5-1. Provisions should be made to supply the Model 75 Data Receiver with 120 vac, 60 cycles, single phase at approximately 8 amperes as power inputs. The Receiver receives a-c power through J18 at the rear of the rack.

5-2. The rack should be installed on a reasonably flat surface and if it is to be installed near a wall, its rear portion should not be less than three feet from the wall. This enables easy access to the rack through the rear door.

5-3. Adjustments and procedures to be executed prior to operating the equipment will be found in CHAPTER IV, OPERATION. Wire size and cable information will be found in CHAPTER VIII, WIRE LIST.

CHAPTER VI

MAINTENANCE

6-1. No special considerations are needed for maintenance of this equipment. However, normal failure of individual components may be expected and can be located through normal maintenance operations. Values of all major component parts used in the chassis are indicated in CHAPTER VII, PARTS LIST. The indicators located on the front of the chassis give indication of malfunction in most cases. By observing these indicators during normal operation, it is possible to determine quickly in which chassis the trouble is located and in which portion of the chassis the trouble is contained. Error detector meters in the 500 Bit Receiver may be used as an aid in determining improper adjustment or equipment failure in the Receiver.

6-2. The only preventive maintenance necessary is the cleaning of the Blower filter approximately once every thirty days. The filter should be removed and cleaned in a solution of warm water and detergent. Periodic tube testing, either with a tube tester or by merely substituting known good tubes, should be carried out. If relays or other electro-mechanical devices do not function properly with normal adjustments, the complete sub-assembly should be replaced and the malfunctioning unit returned to the manufacturer for possible repairs.

6-3. It is strongly urged that this instruction handbook be thoroughly read and completely understood before operating the equipment.

CHAPTER VII

PARTS LIST

ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
1-1				MEC 75-1AA	ASSEMBLY, RACK, DATA RECEIVER	1	
1-2	F1, F2			Bussmann FNM	FUSE, 10 Amp	2	
1-3	I1			Dialight 6S6 DC	LAMP, Incandescent, Bayonet Type 125 V, 6W	1	
1-4	I2			Dialight 6S6 DC	LAMP, Incandescent, Bayonet Type 24V, 6W	1	
1-5	J18			Cannon MS3102A-18-11P	CONNECTOR	1	
				Cannon MS3106B-18-11S	CONNECTOR	1	
				Cannon AN3057-10	CABLE CLAMP	1	
1-6	J19, J20			Cannon MS3102A-22-14P	CONNECTOR	2	
				Cannon MS3106B-22-14S	CONNECTOR	2	
				Cannon AN3057-12	CABLE CLAMP	2	
1-7	P1-P4 DP1-DP4			Cannon MS3102A-14S-5P	CONNECTOR	8	
				Cannon MS3106B-14S-5S	CONNECTOR	8	
				Cannon AN3057-6	CABLE CLAMP	8	
1-8	P5-P8			Switchcraft C-11 -Cont'd.-	JACK	4	
1-8 Cont'd.				Switchcraft 440	PLUG	4	
1-9	S1			Cutler Hammer ST52N	SWITCH, Toggle, 25 Amp, 125V	1	
1-10	S11-S14			Cutler Hammer 7665K4	SWITCH, Toggle, 4DPDT	4	
1-11	TB1			Cinch Jones 2-140	TERMINAL STRIP	1	
1-12	XF1, XF2			Bussmann HPC	FUSE HOLDER	2	
1-13	X11, X12			Dialight 103-3502-1211	INDICATOR HOLDER, Dome Type, Red Lens for S6 Bayonet Type Lamp.	2	

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7 R-4	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
6-1				MEC 75-6B	ASSEMBLY, CONTROL			
6-2	C601, C606 C607 C610-C613 C615 C617-C620 C622			MIL CM-19B-102K	CAPACITOR, Fixed Mica, 1000mmfd, 500vdc, 10% MEC SPN C-13-89	13		
6-3	C602, C604 C609			MIL CM-19B-202K	CAPACITOR, Fixed Mica, 2000mmfd, 500vdc, 10% MEC SPN C-13-11	3		
6-4	C605 C608			Cornell-Dubilier PM4P1	CAPACITOR, Fixed Mylar, 0.1mfd, 400vdc MEC SPN C-03-06	2		
6-5	C614			MIL CM-19B-152K	CAPACITOR, Fixed Mica, 1500mmfd, 500vdc, 10% MEC SPN C-13-42	1		
6-6	C616 C627			Cornell-Dubilier PM4S2	CAPACITOR, Fixed Mylar, .02mfd, 400vdc MEC SPN C-03-11	2		
6-7	C621			Cornell-Dubilier PM6S5	CAPACITOR, Fixed Mylar, .05mfd, 600vdc	1		
6-8	C623			MIL CM-19B-332K	CAPACITOR, Fixed Mica, 3300mmfd, 500vdc, 10% MEC SPN C-13-17	1		
6-9	C624			Fansteel F110-1	CAPACITOR (Blu-Cap), 10mfd, 25vdc MEC SPN C-12-09	1		
6-10	C625			Fansteel F308-1	CAPACITOR (Blu-Cap), 100mfd, 30vdc MEC SPN C-12-07	1		
6-11	C626			G.E. 29F519G4	CAPACITOR, Tantalum, 1mfd, 100vdc MEC SPN C-07-01	1		
6-12	C628			G.E. 29F617G4	CAPACITOR, Tantalum, 2.5mfd, 30vdc	1		
6-13	C603			Cornell-Dubilier PM6D47	CAPACITOR, Fixed Mylar, .0047mfd, 600vdc	1		
6-14	CR601-CR613			CTP503	SEMI-CONDUCTOR DEVICE, DIODE MEC SPN D-01-16	13		
6-15	CR614			1N703	SEMI-CONDUCTOR DEVICE, DIODE, Zener, 3.5V MEC SPN D-01-13	1		
6-16	DS601-DS603			MEC 16-102	INDICATOR, Neon MEC SPN L-01-06	3		
6-17	I601			Eldema 1CF12-4589	LAMP, Incandescent, 24V MEC SPN L-01-01	1		
6-18	K601			C.P. Clare RP7641G8	RELAY (2 Form "C") MEC SPN R-02-08	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
6-19	M601-M604 M606, M608			MEC MN11	CORE, Magnetic	6		
6-20	M605 M607			MEC MN13	CORE, Magnetic	2		
6-21	N601, N603 N605, N606 N608 N612-N614 N616			MEC TN138B	SEMI-CONDUCTOR DEVICE SET	9		
6-22	N602 N611			MEC TN130B	SEMI-CONDUCTOR DEVICE SET	2		
6-23	N604			MEC TN150	SEMI-CONDUCTOR DEVICE SET	1		
6-24	N607, N615 N618, N619			MEC TN58	SEMI-CONDUCTOR DEVICE SET	4		
6-25	N609, N610 N617			MEC TN28	SEMI-CONDUCTOR DEVICE SET	3		
6-26	N620			MEC TN138	SEMI-CONDUCTOR DEVICE SET	1		
6-27	P601			MEC 27-101	PLUG	1		
6-28	R601, R602 R605, R607			MIL RC20GF182K	RESISTOR, Fixed Composition, 1800 Ohms, ±10%, 1/2W	4		
6-29	R603			MIL RC20GF102K	RESISTOR, Fixed Composition, 1K, ±10%, 1/2W	1		
6-30	R604, R609 R618, R619 R623, R625 R628, R632 R634, R637 R641, R650			MIL RC20GF103K	RESISTOR, Fixed Composition, 10K, ±10%, 1/2W	12		
6-31	R606 R646			MIL RC20GF822K	RESISTOR, Fixed Composition, 8200 Ohms, ±10%, 1/2W	2		
6-32	R612, R614 R615, R617 R621, R624 R630, R633 R639, R642			MIL RC20GF472K	RESISTOR, Fixed Composition, 4700 Ohms, ±10%, 1/2W	10		
6-33	R610			MIL RC20GF471K	RESISTOR, Fixed Composition, 470 Ohms, ±10%, 1/2W	1		
6-34	R611			MIL RC20GF473K	RESISTOR, Fixed Composition, 47K, ±10%, 1/2W	1		
6-35	R608 R613			Allen Bradley JA1L040S253UC	POTENTIOMETER, 25K, 2W, Linear Taper MEC SPN P-02-05	2		
6-36	R616			MIL RC20GF242J	RESISTOR, Fixed Composition, 2400 Ohms, ±5%, 1/2W	1		
6-37	R620, R622 R627, R631 R636, R640			MIL RC20GF753J	RESISTOR, Fixed Composition, 75K, ±5%, 1/2W	6		
6-38	R626, R635 R643, R645 R647, R648			MIL RC20GF333K	RESISTOR, Fixed Composition, 33K, ±10%, 1/2W	6		
6-39	R651			MIL RC20GF152K	RESISTOR, Fixed Composition, 1500 Ohms, ±10%, 1/2W	1		
6-40	R629, R638 R644, R649			MIL RC20GF332K	RESISTOR, Fixed Composition, 3300 Ohms, ±10%, 1/2W	4		
6-41	R650			MIL RC20GF153K	RESISTOR, Fixed Composition, 15K, ±10%, 1/2W	1		
6-42	TJ601			Cannon DD-50S	CONNECTOR, Female, 50 Pin Contact, 5 Amp Rating MEC SPN C-11-02	1		
6-43	XI601			Eldema 11H-4593	HOLDER, Indicator MEC SPN L-02-02	1		
6-44	XK601			C.P. Clare RP9005G2	SOCKET, Relay MEC SPN S-03-24	1		
6-45	XM601- XM608			JAN TS103P02	SOCKET, Tube, 9 Pin Miniature MEC SPN S-03-13	8		
6-46	XN601- XN620			JAN TS101P01	SOCKET, Tube, Octal MEC SPN S-03-02	20		
6-47				C.P. Clare RP9006	RETAINER CLIP, Relay Socket MEC SPN S-03-25	1		
6-48				Eldema 11H-4119	LENS CAP (Red) MEC SPN L-02-03	1		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
6-1				MEC 74-6C	ASSEMBLY, Dual 17 Bit shift register	1		
6-2	C601 C603 C604			Fansteel F110-1	CAPACITOR, (Blu-cap) 10µf 25vdc	3		
6-3	C602 C607			Fansteel F308-1	CAPACITOR, (Blu-cap) 100µf 30vdc	2		
6-4	C605 C606			Cornell-Dubilier PM 4S2	CAPACITOR, Fixed Mylar .02µf 400vdc	2		
6-5	CR601			Pacific Semi-Conductor IN703	DIODE, Zener	15.		
6-6	DS601 DS604			MEC 16-102	LAMP, Neon	4		
6-7	M601 M636			MEC MN-13	CORE, Magnetic	2		
6-8	M602 M635			MEC MN-11	CORE, Magnetic	34		
6-9	N601 N604			MEC TN-130B	TRANSISTOR-Network	2		
6-10	N602 N603 N605 N606			MEC TN-51	TRANSISTOR-Network	4		
6-11	P601			Cannon DD-50P	PLUG	1		
6-12	R601 R602 R604 R605			Mil RC20GF273K	RESISTOR, Fixed Composition, 27K ±10%	4		
6-13	R603			Mil RC20GF472K	RESISTOR, Fixed Composition, 4.7K, ±10% 1/2 w	1		
6-14	R606 R607			Mil RC20GF103K	RESISTOR, Fixed composition 10K, ±10% 1/2 w	2		
6-15	S601 S602			OAK 399655-MF	SWITCH, Rotary	2		
6-16	TJ601			Cannon DD-50S	CONNECTOR	1		
6-17	XM601 XM636			Jan TS103PO2	SOCKET, 9 pin miniature mica filled	36		
6-18	XN601 XN606			Jan TS101PO1	SOCKET Octal Mica Filled	6		
6-19				Whitso K-105	SKNOB	2		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
6-1				MEC 74-6C	ASSEMBLY , Dual 17 Bit shift register	1		
6-2	C601 C603 C604			Fansteel F110-1	CAPACITOR, (Blu-cap) 10µf 25vdc	3		
6-3	C602 C607			Fansteel F308-1	CAPACITOR, (Blu-cap) 100µf 30vdc	2		
6-4	C605 C606			Cornell-Dubilier PM 4S2	CAPACITOR, Fixed Mylar .02µf 400vdc	2		
6-5	CR601			Pacific Semi-Conductor IN703	DIODE, Zener	15.		
6-6	DS601 DS604			MEC 16-102	LAMP, Neon	4		
6-7	M601 M636			MEC MN-13	CORE, Magnetic	2		
6-8	M602 M635			MEC MN-11	CORE, Magnetic	34		
6-9	N601 N604			MEC TN-130B	TRANSISTOR-Network	2		
6-10	N602 N603 N605 N606			MEC TN-51	TRANSISTOR-Network	4		
6-11	P601			Cannon DD-50P	PLUG	1		
6-12	R601 R602 R604 R605			Mil RC20GF273K	RESISTOR, Fixed Composition, 27K ±10%	4		
6-13	R603			Mil RC20GF472K	RESISTOR, Fixed Composition, 4.7K, ±10% 1/2 w	1		
6-14	R606 R607			Mil RC20GF103K	RESISTOR, Fixed composition 10K, ±10% 1/2 w	2		
6-15	S601 S602			OAK 399655-MF	SWITCH, Rotary	2		
6-16	TJ601			Cannon DD-50S	CONNECTOR	1		
6-17	XM601 XM636			Jan TS103PO2	SOCKET, 9 pin miniature mica filled	36		
6-18	XN601 XN606			Jan TS101PO1	SOCKET Octal Mica Filled	6		
6-19				Whitso K-105	SKNOB	2		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
4-1				MEC 75-4A	ASSEMBLY, Test Pattern Generator	1		
4-2	C401			Fansteel F308-1	CAPACITOR, (Blu-Cap) 100μf, 30 vdc	1		
4-3	C402 C403 C404 C406 C416 C417			Fansteel F110-1	CAPACITOR, (Blu-Cap) 10μf, 25 vdc	6		
4-4	C405			Mil CM-19B-471K	CAPACITOR, Fixed Mica, 470$\mu\mu$f, ±10% 500 vdc	1		
4-5	C407 C408			Mil CM-19B-152K	CAPACITOR, Fixed Mica, 1500$\mu\mu$f, ±10% 500 vdc	2		
4-6	C409 C410			Mil CM-19B-272K	CAPACITOR, Fixed Mica, 2700$\mu\mu$f, ±10% 500 vdc	2		
4-7	C411 C414			Cornell Dub-ilier PM4S1	CAPACITOR, Fixed Mylar .01μf, 400 vdc	2		
4-8	C413			Mil CM-19B-332K	CAPACITOR, Fixed Mica, 3300$\mu\mu$f, ±10% 500vdc	1		
4-9	CR401 CR402 CR425 CR426			G. E. IN1692	DIODE	4		
4-10	CR404-CR407, CR409 CR410 CR413-CR424			Transitron T12G or Clevite CTP-503	DIODE	18		
4-11	CR408			Pacific Semi-Conductor IN703	DIODE, Zener	1		
4-12	I401			Dialight 6S6-DC	LAMP, Incandescent, 125V, 6w	1		
4-13	K401			Mangecraft 11HPX59	RELAY	1		
4-14	N401			MEC TN-57	TRANSISTOR Network	1		
4-15	N402			MEC TN-138B	TRANSISTOR Network	1		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
4-16	N403			MEC TN-42	TRANSISTOR Network	1		
4-17	N404			MEC TN-28	TRANSISTOR Network	1		
4-18	N405			MEC TN-58	TRANSISTOR Network	1		
4-19	P401			Cannon DD-50P	PLUG, Male, 50 Pin Contact, 5 amp rating	1		
4-20	R420			Mil RC20GF102K	RESISTOR, Fixed composition, 1K, ±10%, 1/2 w	1		
4-21	R402 R407			Mil RC20GF222K	RESISTOR, Fixed composition, 2200Ω ±10% 1/2 w	2		
4-22	R408 R414 R415 R417 R412 R423 R428			Mil RC20GF103K	RESISTOR, Fixed composition, 10K, ±10% 1/2 w	7		
4-23	R405			Mil RC2-GF223K	RESISTOR, Fixed composition, 22K ±10% 1/2 w	1		
4-24	R406 R422			Mil RC20GF472K	RESISTOR, Fixed composition, 4700Ω, ±10% 1/2 w	2		
4-25	R410 R427			Mil RC20GF332K	RESISTOR, Fixed composition, 3300Ω ±10% 1/2 w	2		
4-26	R416			Mil RC20GF182K	RESISTOR, Fixed Composition, 1800Ω ±10% 1/2w	1		
4-27	R409 R424 R413			Mil RC20GF333K	RESISTOR, Fixed composition, 33K, ±10% 1/2 w	3		
4-28	R429			Mil RC42GF101J	RESISTOR, Fixed composition, 100Ω ±5% 2 w	1		
4-29	R407 R421			Mil RC20GF473K	RESISTOR, Fixed composition, 47K, ±10% 1/2w	2		
4-30	S401			Centralab PA-2011	SWITCH, Rotary, Non-shorting, 4 pole 2-6 positions	1		
4-31	S402			Micro 2PB11	SWITCH, Pushbutton	1		
4-32	TJ401			Cannon DD-50S	CONNECTOR, Female, 50 pin contact, 5 amp rating	1		
4-33	XI401			Dialight 103=3502-1211	INDICATOR holder, Dome type, red lens for Bayonet Lamp	1		
4-34	XK401 XN401-XN405			Jan TS101P01	SOCKET, Octal, Mica Filled	6		
4-35				Whitso K-105	KNOB	1		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
5-1				MEC 75-5A	ASSEMBLY, SWITCHOVER	1		
5-2	CR501-CR507			G. E. IN1692	DIODE	7		
5-3	F501			Bussmann MDA	FUSE, 1 Amp.	1		
5-4	I501-I505			Dialight Corp. 686-DC	LAMP, Incandescent, Bayonet Base, 125V 6W	5		
5-5	K501-K508			Magnecraft 11HPX-59	RELAY	8		
5-6	MV501 MV502			Assembly Prod. 261-C	METER, Relay, with double adjustable contacts for low and high detection, 1 ma. coil, 60 division scale with 13 major subdivisions marked at alternate major divisions as follows - 0, 20, 40, 60, 80, 100, 120 with 120 at full scale mark. Contacts rated up to 25 ma. dc at 125 vdc.	2		
5-7	N501			MEC TN-57	TRANSISTOR NETWORK	1		
5-8	P501			Cannon DD-50P	PLUG	1		
5-9	R501			Phaostron CA4RS-1/2	RESISTOR, Precision, 14.3K. ± 1%, 1/2W or IRC equivalent	1		
5-10	R502			Phaostron CA4RS-1/2	RESISTOR, Precision, 23.9K. ± 1%, 1/2W or IRC equivalent	1		
5-11	R503			MIL RC32GF202K	RESISTOR, Fixed Composition, 2000 ohm ± 10%, 1W	1		
5-12	R504			MIL RC32GF332K	RESISTOR, Fixed Composition, 3300 ohm ± 10%, 1W	1		
5-13	R505 R506			MIL RC20GF471K	RESISTOR, Fixed Composition, 470 ohm ± 10%, 1/2 W	2		
5-14	R507			MIL RC32GF182J	RESISTOR, Fixed Composition, 1800 ohm ± 5%, 1W	1		
5-15	R508			MIL RC20GF182K	RESISTOR, Fixed Composition, 1800 ohm ± 10%, 1/2W	1		
5-16	R509			MIL RC20GF473K	RESISTOR, Fixed Composition, 47K, ± 10%, 1/2W	1		
5-17	R510			MIL RC42GF221J	RESISTOR, Fixed Composition, 220 ohm ± 5%, 2W	1		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
5-18	R511			MIL RC32GF101K	RESISTOR, Fixed Composition, 100 ohm ± 10%, 1W	1		
5-19	R512			Ward Leonard 25F2	RESISTOR, Fixed Wire Wound, 2 ohm ± 5%, 25W or Ohmite equal	1		
5-20	S501			Micro 2PB11	SWITCH, Pushbutton	1		
5-21	XF501			Bussmann HKP	FUSE HOLDER	1		
5-22	XI501			Dialight Corp. 103-3502-1212	INDICATOR HOLDER, Dome Type, Green Lens, for S6 Bayonet Lamp	1		
5-23	XI502 XI503			Dialight Corp. 103-3502-1216	INDICATOR HOLDER, Dome Type, Yellow Lens, for S6 Bayonet Lamp	2		
5-24	XI504 XI505			Dialight Corp. 103-3502-1211	INDICATOR HOLDER, Dome Type, Red Lens, for S6 Bayonet Lamp	2		
5-25	XN501 XK501-XK508			JAN TS101P01	SOCKET, Octal Mica Filled	9		
5-26	R513			Mil RC42GF331K	RESISTOR, fixed composition 330Ω ±10%, 2w	1		
7-1				MEC 72-7B	ASSEMBLY, POWER CONTROL	1		
7-2	CR701-CR709			G.E. IN1695	DIODE	9		
7-3	DS701-DS709			Eldema 1CG12-4535	LAMP, Neon to Spec. 21C-3864-7	9		
7-4	I701-I702			Eldema 1GF-4976	LAMP, Incandescent, (Red)	2		
7-5	MV701			Beede E-25	METER, 1.2 MA, (Scale 0-12) Horizontal Mounting.	1		
7-6	P701			Cannon DD-50P	PLUG	1		
7-7	R701			MIL RC20GF393K	RESISTOR, Fixed composition, 39K ±10% 1/2W	1		
7-8	R702			I.R.C. DCC	RESISTOR, Precision, 54K ±1% 1/2W	1		
7-9	R703			I.R.C. DCC	RESISTOR, Precision, 12K ±1% 1/2W	1		
7-10	R704			I.R.C. DCC	RESISTOR, Precision, 20K ±1% 1/2W	1		
7-11	R705			I.R.C. DCC	RESISTOR, Precision, 85K ±1% 1/2W	1		
7-12	R706, R707 R709-R722			MIL RC20GF104K	RESISTOR, Fixed composition, 100K ±10% 1/2W	16		
7-13	R708			I.R.C. DCC	RESISTOR, Precision, 250K ±1% 1/2W	1		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
7-14	R723			MIL RC42GF820K	RESISTOR, Fixed composition, 82Ω ±10% 2W	1		
7-15	S701			Cutler Hammer ST52N	SWITCH, Toggle, DPDT	1		
7-16	S702			Oak 399655-MF	SWITCH, Rotary	1		
7-17	XDS701-XDS709			Eldema 11H-4593	INDICATOR HOLDER	9		
7-18				Whitso K-150	KNOB	1		
7-19				Eldema 11H-4110	LENS CAP, (Translucent)	1		
7-20				Eldema 11H-4119	LENS CAP, (Red)	8		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
1				McLean 2EB508C	ASSEMBLY, BLOWER	1		
8-1				MEC 71-8A	ASSEMBLY, Data Line Amplifier	1		
8-2	C801 C803			Cornell Dubilier PM 4S1	CAPACITOR, Fixed Mylar, .01μf, 400 vdc	2		
8-3	C826 C827			Cornell Dubilier PM 4S2	CAPACITOR, Fixed Mylar, .02μf, 400 vdc	2		
8-4	C811-C814			Cornell Dubilier PM4P1	CAPACITOR, Fixed Mylar, .1μf, 400 vdc	4		
8-5	C802 C837			Cornell Dubilier PM6D5	CAPACITOR, Fixed Mylar, .005μf, 600 vdc	2		
8-6	C804 C805 C815			Cornell Dubilier PM2P47	CAPACITOR, Fixed Mylar, .47 μf, 200 vdc	3		
8-7	C824			Cornell Dubilier PM4S5	CAPACITOR, Fixed Mylar, .05μf, 400 vdc	1		
8-8	C806			Mil CM-19B-501K	CAPACITOR, Fixed Mica, 500$\mu\mu$f, 500 vdc ±10%	1		
8-9	C807 C809 C810			Mil CM-19B-202K	CAPACITOR, Fixed Mica, 2000$\mu\mu$f, 500 vdc ±10%	3		

1 ITEM NO.	2 REFER. DESIG-NATOR	3 CLASS	3 STOCK NO.	4 MFG. AND PART NO.	5 DESCRIPTION 1 2 3 4 5 6 7	6 UNIT PER ASSY.	7 PROCURE-MENT CODE	8 UNIT COST (EST.)
8-10	C817-C819 C821 C825 C828			Mil CM-19B-101K	CAPACITOR, Fixed Mica, 100$\mu\mu$f ±10%, 500 vdc	6		
8-11	C816			Mil CM-19B-501K	CAPACITOR, Fixed Mica, 500 $\mu\mu$f ±10% 500 vdc	1		
8-12	C820			Mil CM-19B=152K	CAPACITOR, Fixed Mica, 1500 $\mu\mu$f, ±10% 500 vdc	1		
8-13	C829-C831			Mil CM-19B-560K	CAPACITOR, Fixed Mica, 56 $\mu\mu$f, ±10%, 500 vdc	3		
8-14	C808 C832 C833			Aerovox AEP8J	CAPACITOR, Fixed 40 μf, 450 v, Plug-in	3		
8-15	C834			Aerovox AEP88J	CAPACITOR, Fixed, 40-40μf, 450 v, Dual Plug In	1		
8-16	C822			Mil CM-19B=102K	CAPACITOR, Fixed Mica, 1000 $\mu\mu$f, ±10% 500vdc	1		
8-17	C823			Mil CM-19B-471K	CAPACITOR, Fixed Mica, 470$\mu\mu$f, ±10% 500 vdc	1		
8-18	C835			Mil CM-19B-470K	CAPACITOR, Fixed Mica, 47$\mu\mu$f, ±10% 500 vdc	1		
8-19	CR801-CR804 CR809-CR815			Hughes HD6227	DIODE	11		
8-20	CR816-CR824			G. E. IN1695	DIODE	9		
8-21	CR805-CR808			Pacific Semi-Conductor PC 030	DIODE	4		
8-22	F801			Bussmann AGC	FUSE, 1 amp	1		
8-23	DS801-DS804			Eldema ICG12-4535	LAMP, Neon to Spec. 21C-3864-7	4		
8-24	L801 L802			UTC MQA-17	INDUCTOR, 10 hy, 7 ma. max.	2		
8-25	L803			UTC HVC-8	INDUCTOR	1		
8-26	P801			Cannon DD-50P	PLUG, Male, 50 Pin contact, 5 amp. rating	1		
8-27	R802			Mil RC20GF434J	RESISTOR, Fixed Composition, 430K, ±5% 1/2 w	1		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
8-28	R803 R809 R811 R820 R821			Mil RC20GF244J	RESISTOR, Fixed composition, 240K, ±5% 1/2 w	5		
8-29	R805 R883 R823 R825 R826 R829 R831 R834- R837 R861 R866 R877 R880 R881 R854			Mil RC20GF104K	RESISTOR, Fixed Composition, 100K, ±10% 1/2 w	17		
8-30	R806 R830 R859			Mil RC20GF563K	RESISTOR, Fixed Composition, 56K, ±10%, 1/2 w	3		
8-31	R807 R862 R865			Mil RC20GF124K	RESISTOR, Fixed composition, 120K, ±10% 1/2 w	3		
8-32	R815 R819			Mil RC20GF224K	RESISTOR, Fixed composition, 220K, ±10% 1/2 w	2		
8-33	R816			Mil RC20GF102K	RESISTOR, Fixed composition, 1K ±10% 1/2 w	1		
8-34	R817 R818 R833 R868 R869 R871			Mil RC20GF624J	RESISTOR, Fixed composition, 62K ±5% 1/2 w	6		
8-35	R828 R839 R845 R851			Mil RC20GF204J	RESISTOR, Fixed composition, 200K, ±5% 1/2 w	4		
8-36	R832 R838 R844 R850 R863 R864 R867 R870 R872			Mil RC20GF624J	RESISTOR, Fixed composition, 620 K ±5% 1/2 w	9		
8-37	R855			Mil RC20GF824K	RESISTOR, Fixed composition, 820K ±10% 1/2 w	1		

1	2	3		4	5	6	7	8
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE	UNIT COST (EST.)
8-38	R857			Mil RC20GF333K	RESISTOR, Fixed composition, 33K ±10%, 1/2 w	1		
8-39	R810			Mil RC20GF202J	RESISTOR, Fixed composition 2K, ±5% 1/2 w	1		
8-40	R808 R856 R858			Mil RC20GF105K	RESISTOR, Fixed composition, 1M ±10% 1/2 w	3		
8-41	R824 R827			Mil RC20GF124K	RESISTOR, Fixed composition, 1.2M, ±10% 1/2 w	2		
8-42	R860			Mil RC20GF222K	RESISTOR, Fixed composition, 2.2K, ±10% 1/2 w	1		
8-43	R814			Mil RC42GF222K	RESISTOR, Fixed composition, 2.2K, ±10% 2 w	1		
8-44	R840 R841 R846 R847 R852 R853			Mil RC42GF433J	RESISTOR, Fixed composition, 43K, ±5%, 2 w	6		
8-45	R842			Mil RC20GF205J	RESISTOR, Fixed composition, 2M, ±5% 1/2 w	1		
8-46	R873 R874			Mil RC42GF101K	RESISTOR, Fixed composition 100Ω ±10% 2W	2		
8-47	R879			Mil RC42GF511J	RESISTOR, Fixed composition, 510Ω ±5% 2 w	1		
8-48	R875			Ward Leonard 10F8000	RESISTOR, Fixed, wire wound 8K, 10w	1		
8-49	R878			Ward Leonard 10F3000	RESISTOR, Fixed, wire wound 3K, 10w	1		
8-50	R876			Mil RC42GF202J	RESISTOR, Fixed composition, 2K, ±5%, 2 w	1		
8-51	R849 R843			Allen Bradley JAIL 040S255UC	POTENTIOMETER, 2.5M 2w, Linear Taper	2		
8-52	R822			Allen Bradley JAIL040S503UC	POTENTIOMETER, 50K, 2w, Linear Taper	1		
8-53	R801			Allen Bradley JAIL040S104UC	POTENTIOMETER, 100K, 2W Linear taper	1		
8-54	R804			Mil RC20GF271K	RESISTOR, Fixed Composition 270Ω ±10% 1/2 w	1		
8-55	R812			Mil RC20GF432K	RESISTOR, Fixed composition, 4.3K, ±10% 1/2 w	1		
8-56	R813			Mil RC20GF473K	RESISTOR, Fixed composition, 47K, ±10% 1/2 w	1		
8-57	R848			Mil RC20GF105J	RESISTOR, Fixed composition, 1M, ±5% 1/2 w	1		
8-58	R882			Mil RC20GF433K	RESISTOR, Fixed composition, 43K, ±10% 1/2 w	1		

ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
6-17	N601 N603 N604 N611 N612 N616- N618			MEC TN-138B	TRANSISTOR, Network	8	
6-18	N602			MEC TN-150	TRANSISTOR Network	1	
6-19	N605 N613- N615			MEC TN-58	TRANSISTOR Network	4	
6-20	N606			MEC TN-130B	TRANSISTOR Network	1	
6-21	N607- N610			MEC TN-28	TRANSISTOR Network	4	
6-22	P601			Cannon DD-50P	PLUG, Male, 50 Pin contact, 5 amp. rating	1	
6-23	R601			Mil RC20GF102K	RESISTOR fixed composition, 1000Ω ±10%, 1/2 w	1	
6-24	R602 R604 R606 R615 R627 R629 R636 R638 R641 R643			Mil RC20GF103K	RESISTOR, Fixed Composition, 10K, ±10% 1/2 w	10	
6-25	R603 R610 R611 R651			Mil RC20GF182K	RESISTOR, Fixed Compositinn, 1800Ω ±10% 1/2 w	4	
6-26	R605 R613 R614 R618 R621 R624 R628 R621 R624 R628 R630 R631 R637 R639 R642 R644 R646 R647 R649			Mil RC20GF472K	RESISTOR, Fixed Composition, 4700Ω ±10% 1/2 w	16	

1	2	3		4	5	6	7
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
4-1				MEC 165-4C	ASSEMBLY, POWER SUPPLY	1	
4-2	C401 C402 C421-C423			Mallory 20-71937	CAPACITOR, Computer Grade, 4000μf 60 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	5	
4-3	C403 C425 C443 C444			Cornell Dubilier PM4S1	CAPACITOR, Fixed, Mylar, .01μf 400 vdc	4	
4-4	C424			Cornell Dubilier PM4P1	CAPACITOR, Fixed, Mylar, .1μf 400 vdc	1	
4-5	C404 C426			Fansteel F308-1	CAPACITOR, Blu-cap, 100μf 30 vdc	2	
4-6	C441 C442			Mallory 20-71855	CAPACITOR, Computer Grade, 2000μf 100 vdc, 2-1/16 x 4-1/2, Alum. can with acetate sleeve.	2	
4-7	C445			Fansteel F316-1	CAPACITOR, Blu-cap, 30μf 100 vdc	1	
4-8	CR401 CR421			G. E. 4JA211AB1AC2	RECTIFIER	3	
4-9	CR402 CR422			International Rectifier IN1519	DIODE, Zener (1Z4.7)	2	
4-10	CR442			International Rectifier IN1524	DIODE, Zener (1Z12)	1	
4-11	F401 F403			Bussmann AGC	FUSE, 1 Amp	2	
4-12	F402			Bussmann AGC	FUSE, 3 Amp	1	
4-13	F404			Bussmann MDX	FUSE, Fusetron, Slo-Blow, 3 Amp.	1	
4-14	P401			Cannon DD-50P	PLUG	1	
4-15	Q423 Q442			Delco 2N553	TRANSISTOR, (Mount with Parts #100 & #101)	2	
4-16	Q401 Q421 Q441 Q422			Delco 2N443	TRANSISTOR, (Lug type Leads)	4	
4-17	Q402 Q403 Q424 Q443			G. E. 2N525	TRANSISTOR	4	
4-18	Q404 Q425 Q444			Sylvania 2N377A	TRANSISTOR	3	
4-19	R401, R402 R421A R421B R441 R442			Ward Leonard 5X1	RESISTOR, Axiohm, 1Ω 5W	6	
4-20	R403 R443			Ward Leonard 5X2	RESISTOR, Axiohm, 2Ω 5W	2	
4-21	R404 R425 R444			MIL RC42GF102K	RESISTOR, Fixed composition, 1K ±10% 2W	3	

1	2	3		4	5	6	7
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
4-22	R405			MIL RC42GF151K	RESISTOR, Fixed composition, 150Ω ±10% 2W	1	
4-23	R406			MIL RC20GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1/2W	1	
4-24	R407 R428 R447			MIL RC20GF101K	RESISTOR, Fixed composition, 100Ω ±10% 1/2W	3	
4-25	R408			MIL RC20GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1/2W	1	
4-26	R409 R430 R449			MIL RC20GF822K	RESISTOR, Fixed composition, 8.2K ±10% 1/2W	3	
4-27	R410 R431 R450			MIL RC20GF621J	RESISTOR, Fixed composition, 620Ω ±5% 1/2W	3	
4-28	R411 R432			MIL RC20GF472K	RESISTOR, Fixed composition, 4.7K ±10% 1/2W	2	
4-29	R412			MIL RC32GF121K	RESISTOR, Fixed composition, 120Ω ±10% 1W	1	
4-30	R414 R435			Chicago Tel. RA20LASB250A	POTENTIOMETER, 25Ω 2W	2	
4-31	R415			MIL RC32GF820J	RESISTOR, Fixed composition, 82Ω ±5% 1W	1	
4-32	R413			MIL RC42GF131J	RESISTOR, Fixed composition, 130Ω ±5% 2W	1	
4-33	R422			Ward Leonard 10F1	RESISTOR, Fixed, Wire wound, 1Ω 10W	1	
4-34	R423 R424			Ward Leonard 10F2	RESISTOR, Fixed, Wire wound, 2Ω 10W	2	
4-35	R426 R437			Ward Leonard 10F150	RESISTOR, Fixed, Wire wound, 150Ω 10W	2	
4-36	R427 R446			MIL RC32GF681K	RESISTOR, Fixed composition, 680Ω ±10% 1W	2	
4-37	R429 R448			MIL RC32GF122K	RESISTOR, Fixed composition, 1.2K ±10% 1W	2	
4-38	R433 R416			MIL RC42GF271K	RESISTOR, Fixed composition, 270Ω ±10% 2W	2	
4-39	R436			MIL RC32GF510J	RESISTOR, Fixed composition, 51Ω ±5% 1W	1	
4-40	R434			MIL RC42GF181J	RESISTOR, Fixed composition, 180Ω ±5% 2W	1	
4-41	R451			MIL RC42GF302J	RESISTOR, Fixed composition, 3K ±5% 2W	1	
4-42	R453			Allen Bradley JLU-1011 or JA1L040S101UC	POTENTIOMETER, 100Ω 2W, Linear Taper	1	
4-43	R454			MIL RC42GF272J	RESISTOR, Fixed composition, 2.7K ±5% 2W	1	
4-44	R455			Ward Leonard 5X500	RESISTOR, Fixed, Axiohm, 500Ω 5W	1	
4-45	R452			MIL RC32GF561J	RESISTOR, Fixed composition, 560Ω ±5% 1W	1	
4-46	R445			Ward Leonard 10F250	RESISTOR, Fixed, Wire wound, 250Ω 10W	1	
4-47	T401			TTI 5486	TRANSFORMER	1	

1	2	3		4	5	6	7
ITEM NO.	REFER. DESIG-NATOR	CLASS	STOCK NO.	MFG. AND PART NO.	DESCRIPTION 1 2 3 4 5 6 7	UNIT PER ASSY.	PROCURE-MENT CODE
4-48	TJ401-TJ404			H. H. Smith 221	JACK, Midget Banana (Black)	4	
4-49	XF401-XF404			Bussmann HKP	FUSEHOLDER	4	

CHAPTER VIII

WIRE LIST

DRAWN | CHECKED | REVIEWED | DATE APPROVED FOR MFG. | REVISIONS | INDEX

WIRE NO.	REFERENCE TERMINAL	PAGE DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	J1	4		Data Line Amplifier #1		
	J2	6		Data Line Amplifier #2		
	J3	8		Data Line Amplifier #3		
	J4	10		Data Line Amplifier #4		
	J5	12		Control Chassis #1		
	J6	14		Control Chassis #2		
	J7	16		Control Chassis #3		
	J8	18		Control Chassis #4		
	J9	20		Power Switchover		
	J10	22		Test Pattern Generator		
	J11	24		Power Control		
	J12	26		Dual 17 Bit S.R. #1		
	J13	28		Dual 17 Bit S.R. #2		
	J14	30		Dual 17 Bit S.R. #3		
	J15	32		Dual 17 Bit S.R. #4		
	J16	34		Power Supply (A)		
	J17	36		Power Supply (B)		
	J18	38		Power Input Connector		
	J19	39		Output Connector (A)		
	J20	40		Output Connector (B)		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 1 OF 66 SHEETS

DRAWN | CHECKED | REVIEWED | DATE APPROVED FOR MFG. | REVISIONS | INDEX

WIRE NO.	REFERENCE TERMINAL	PAGE DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	DP1	41		Dummy Plug #1		
	DP2	42		Dummy Plug #2		
	DP3	43		Dummy Plug #3		
	DP4	44		Dummy Plug #4		
	P1	45		Data Line #1 Input Conn.		
	P2	46		Data Line #2 Input Conn.		
	P3	47		Data Line #3 Input Conn.		
	P4	48		Data Line #4 Input Conn.		
	P5	49		Recording Output #1		
	P6	50		Recording Output #2		
	P7	51		Recording Output #3		
	P8	52		Recording Output #4		
	L1	53		Power Available Lamp		
	L2	54		Test Playback Lamp		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 2 OF SHEETS

DRAWN | DATE APPROVED FOR MFG. | INDEX

CHECKED | REVISIONS 1

REVIEWED

WIRE NO.	REFERENCE TERMINAL	PAGE DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	-85V Buss	55		-85V Distribution		
	-20V Buss	56		-20V Distribution		
	0V Buss	57		0V Distribution		
	+12V Buss	58		+12V Distribution		
	F1	59		Line Fuse		
	S1	60		Line Switch		
	TB1	61		A.C. Terminal Board		
	BWR	62		Blower		
1	S11	63		Operate Simulate Switch		
1	S12	64		Operate Simulate Switch		
1	S13	65		Operate Simulate Switch		
1	S14	66		Operate Simulate Switch		

NOTE: Cable # 1 is Power Cable
Cable # 2 is Signal Cable

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A75WL1A | SHEET 3 OF SHEETS

DRAWN

CHECKED | DATE APPROVED FOR MFG.

REVIEWED | REVISIONS 1

J1
DATA LINE AMPLIFIER #1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J5-3	2	1KC Output	22	BR
	8					
	9	J5-2	2	EOW Output	22	O
	10					
	11					
	12					
	13	J5-1	2	Data Output	22	G
	14					
	15	S11 - A2	2	Input To DLA	*	
	16					
	17	S11 -B2	2	Input To DLA RET.	*	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES: *RG-174/U Coax,
Ground each coax shield at only one end.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A75WL1A | SHEET 4 OF SHEETS

Rev. 6/15/61

DRAWN	DATE APPROVED FOR MFG.	J1 DATA LINE AMPLIFIER #1
CHECKED		
REVIEWED	REVISIONS	

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J2 -34	1	AC Switched	18*	W-S
	35					
	36					
	37	J2 -36	1	AC Common	18*	W
	38	J11- 22	1	-250V	22	Y
	39	J11- 18	1	+250V	22	W-R
	40					
	41					
	42					
	43					
	44					
	45	OV- 14	1	OV	20	BK
	46	P5 -2	2	Recorder Return	22	BK
	47					
	48					
	49	P5 -1	2	Output to Recorder	#	
	50	CH Gnd		Chassis Ground		

NOTES: *- #18 Twisted Pair
#- RG-174/U Coax,
Ground each coax shield at only one end.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 5 OF SHEETS

DRAWN	DATE APPROVED FOR MFG.	J2 DATA LINE AMPLIFIER #2
CHECKED		
REVIEWED	REVISIONS 1	

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J6-3	2	1KC Output	22	BR
	8					
	9	J6-2	2	EOW Output	22	O
	10					
	11					
	12					
	13	J6-1	2	Data Output	22	G
	14					
	15	S12-A2	2	Input To DLA	*	
	16					
	17	S12-B2	2	Input To DLA RET.	*	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES: *RG -174/U Coax,
Ground each coax Shield at only one end.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 6 OF SHEETS

Rev. 6/15/61

DRAWN	DATE APPROVED FOR MFG.	J2
CHECKED		
REVIEWED	REVISIONS	DATA LINE AMPLIFIER #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J1-34	1	AC Switched	18*	W-S
	35	J3-34	1	AC Switched	18*	W-S
	36	J1-37	1	AC Common	18*	W
	37	J3-36	1	AC Common	18*	W
	38	J11-23	1	-250V	22	Y
	39	J11-19	1	+250V	22	W-R
	40					
	41					
	42					
	43					
	44					
	45	OV-15	1	OV	20	BK
	46	P6-2	2	Recorder Return	22	BK
	47					
	48					
	49	P6-1	2	Output to Recorder	#	
	50	Ch. Gnd.		Chassis Ground		

NOTES: *- #18 Twisted Pair
#- RG-174/U Coax
Ground each coax shield at only one end.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 7 OF SHEETS

DRAWN	DATE APPROVED FOR MFG.	J3
CHECKED		
REVIEWED	REVISIONS 1	

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J7-3	2	1KC Output	22	BR
	8					
	9	J7-2	2	EOW Output	22	O
	10					
	11					
	12					
	13	J7-1	2	Data Output	22	G
	14					
	15	S13-A2	2	Input To DLA	*	
	16					
	17	S13-B2	2	Input To DLA RET.	*	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES: *RG-174/U Coax,
Ground each coax shield at only one end.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 8 OF SHEETS

Rev. 6/15/61

DRAWN	DATE APPROVED FOR MFG.	J3
CHECKED		
REVIEWED	REVISIONS	DATA LINE AMPLIFIER #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J2-35	1	AC Switched	18*	W-S
	35	J4-34	1	AC Switched	18*	W-S
	36	J2-37	1	AC Common	18*	W
	37	J4-36	1	AC Common	18*	W
	38	J11-24	1	-250V	22	Y
	39	J11-20	1	+250V	22	W-R
	40					
	41					
	42					
	43					
	44					
	45	0V-7	1	0V	20	BK
	46	P7-2	2	Recorder Return	22	BK
	47					
	48					
	49	P7-1	2	Output to Recorder	#	
	50	Ch. Gnd.		Chassis Ground		

NOTES: *-#18 Twisted Pair
#- RG-174/U Coax
Ground each coax shield at only one end.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 9 OF SHEETS

DRAWN	DATE APPROVED FOR MFG.	J4
CHECKED		
REVIEWED	REVISIONS 1	DATA LINE AMPLIFIER #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3					
	4					
	5					
	6					
	7	J8-3	2	1KC Output	22	BR
	8					
	9	J8-2	2	EOW Output	22	O
	10					
	11					
	12					
	13	J8-1	2	Data Output	22	G
	14					
	15	S14-A2	2	Input To DLA	*	
	16					
	17	S14-B2	2	Input to DLA RET=	*	
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES: *RG-174/U Coax,
Ground each coax shield at only one end

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 10 OF SHEETS

Rev. 6/15/61

DRAWN | DATE APPROVED FOR MFG. | J4
CHECKED | DATA LINE AMPLIFIER #4
REVIEWED | REVISIONS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J3-35	1	AC Switched	18*	W-S
	35	J10-36	1	AC Switched	18*	W-S
	36	J3-37	1	AC Common	18*	W
	37	J10-34	1	AC Common	18*	W
	38	J11-25	1	-250V	22	Y
	39	J11-21	1	+250V	22	W-R
	40					
	41					
	42					
	43					
	44					
	45	0V-6	1	0V	20	BK
	46	P8-2	2	Recorder Return	22	BK
	47					
	48					
	49	P8-1	2	Output to Recorder	#	
	50	Ch. Gnd.		Chassis Ground		

NOTES: *- #18 Twisted Pair
#- RG-174/U Coax
Ground each coax shield at only one end.

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 11 OF SHEETS

DRAWN | DATE APPROVED FOR MFG. | J5
CHECKED | CONTROL CHASSIS #I
REVIEWED | REVISIONS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1 -13	2	Data From D.L.A.	22	G
	2	J1 -9	2	EOW From D.L.A.	22	O
	3	J1 -7	2	1KC From D.L.A.	22	BR
	4	J12-10	2	Data "B" From S.R.	22	Y
	5					
	6	J12-8	2	EOW "A" From S.R.	22	BL
	7					
	8	J12-11	2	Data "A" From S.R.	22	V
	9					
	10	J12-9	2	EOW "B" From S.R.	22	W
	11					
	12	J12-4	2	Data to S.R.	22	W-BR
	13	J19-B	2	Copy to "A" Reg	22	BR
	14	J20-B	2	Copy to "B" Reg	22	BR
	15	J20-C	2	EOW to "B" Reg	22	O
	16	J20-A	2	Data to "B" Reg	22	W-BL
	17	J19-C	2	EOW To "A" Reg	22	O
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 12 OF SHEETS

DRAWN	DATE APPROVED FOR MFG.	J 5
CHECKED		CONTROL CHASSIS #1
REVIEWED	REVISIONS	

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J19-A	2	Data to "A" Reg	22	W-BL
	35	J12-7	2	EOW to S.R.	22	W-R
	36	J12-1	2	C.D. Trigger to S.R	22	W-O
	37					
	38	J10-9	2	Test Data	22	W-V
	39	J10-5	2	Test EOW	22	W-O
◇1	40 ----			Test Gate (-20V)		
	41	J10-1	2	Test I/O	22	O
	42					
	43---	12V-7	1	+12V	22	R
	44---					
	45---	0V-17	1	0V	20	BK
	46---					
◇1	47---→	20V-9	1	-20V	22	S
	48---↓					
	49	85V-6	1	-85V	22	W-BK
	50	Ch.Gnd		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 13 OF SHEETS

DRAWN	DATE APPROVED FOR MFG.	J6
CHECKED		CONTROL CHASSIS #2
REVIEWED	REVISIONS	

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J2-13	2	Data From D.L.A.	22	G
	2	J2-9	2	EOW From D.L.A.	22	O
	3	J2-7	2	1KC From D.L.A.	22	BR
	4---┐	J13-10	2	Data "B" From S.R.	22	Y
	5---┘					
	6---┐	J13-8	2	EOW "A" From S.R.	22	BL
	7---┘					
	8---┐	J13-11	2	Data "A" From S.R.	22	V
	9---┘					
	10---┐	J13-9	2	EOW "B" From S.R.	22	W
	11---┘					
	12	J13-4	2	Data to S.R.	22	W-BR
	13	J19-E	2	Copy to "A" Reg	22	G
	14	J20-E	2	Copy to "B" Reg	22	G
	15	J20-F	2	EOW to "B" Reg	22	BL
	16	J20-D	2	Data to "B" Reg	22	Y
	17	J19-F	2	EOW To "A" Reg	22	BL
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 14 OF SHEETS

Rev. 6/15/61

DRAWN | CHECKED | REVIEWED | DATE APPROVED FOR MFG. | REVISIONS

J 6
CONTROL CHASSIS #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J19-D	2	Data to "A" Reg	22	Y
	35	J13-7	2	EOW to S.R.	22	W-R
	36	J 3-1	2	C.D. Trigger to S.R	22	W-O
	37					
	38	J10-10	2	Test Data	22	W-S
	39	J10-6	2	Test EOW	22	W-Y
	40	J10-13	2	Test Gate	22	V
	41	J10-2	2	Test I/O	22	BL
	42					
	43--- 44---	12V-9	1	+12V	22	R
	45--- 46---	0V-19	1	0V	20	BK
	47--- 48---	20V-11	1	-20V	22	S
	49	85V-8	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 15 OF SHEETS

DRAWN | CHECKED | REVIEWED | DATE APPROVED FOR MFG. | REVISIONS

J 7
CONTROL CHASSIS #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-13	2	Data From D.L.A.	22	G
	2	J3-9	2	EOW From D.L.A.	22	O
	3	J3-7	2	1KC From D L.A.	22	BR
	4--- 5---	J14-10	2	Data "B" From S.R.	22	Y
	6--- 7---	J14-8	2	EOW "A" From S.R.	22	BL
	8--- 9---	J14-11	2	Data "A" From S.R.	22	V
	10--- 11---	J14-9	2	EOW "B" From S.R.	22	W
	12	J14-4	2	Data to S.R.	22	W-BR
	13	J19-H	2	Copy to "A" Reg	22	W-BR
	14	J20-H	2	Copy to "B" Reg	22	W-BR
	15	J20-J	2	EOW to "B" Reg	22	W-R
	16	J20-G	2	Data to "B" Reg	22	V
	17	J19-J	2	EOW To "A" Reg	22	W-R
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 16 OF SHEETS

J7

CONTROL CHASSIS #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J19- G	2	Data to "A" Reg	22	V
	35	J14-7	2	EOW to S.R.	22	W-R
	36	J14-1	2	C.D. Trigger to S.R	22	W-O
	37					
	38	J10- 11	2	Test Data	22	BK
	39	J10- 7	2	Test EOW	22	W-G
	40	J10- 14	2	Test Gate	22	O
	41	J10- 3	2	Test I/O	22	V
	42					
	43--- 44---	12V- 3	1	+12V	22	R
	45--- 46---	0V- 4	1	0V	20	BK
	47--- 48---	20V- 4	1	-20V	22	S
	49	85V- 2	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

J 8

CONTROL CHASSIS # 4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J 4 -13	2	Data From D.L.A.	22	G
	2	J 4 -9	2	EOW From D.L.A.	22	O
	3	J 4 -7	2	1KC From D.L.A.	22	BR
	4--- 5---	J15-10	2	Data "B" From S/R.	22	Y
	6--- 7---	J 15-8	2	EOW "A" From S.R.	22	BL
	8--- 9---	J 15-11	2	Data "A" From S.R.	22	V
	10- 11--	J 15-9	2	EOW "B" From S.R.	22	W
	12	J15-4	2	Data to S.R.	22	W-BR
	13	J19-L	2	Copy to "A" Reg	22	W-Y
	14	J20-L	2	Copy to "B" Reg	22	W-Y
	15	J20-M	2	EOW to "B" Reg	22	W-G
	16	J20-K	2	Data to "B" Reg	22	W-O
	17	J19-M	2	EOW To "A" Reg	22	W-G
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J8

CONTROL CHASSIS #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J19-K	2	Data to "A" Reg	22	W-O
	35	J15-7	2	EOW to S.R.	22	W-R
	36	J15-1	2	C.D. Trigger to S.R	22	W-O
	37					
	38	J10-12	2	Test Data	22	BL
	39	J10- 8	2	Test EOW	22	W-BL
	40	J10- 15	2	Test Gate	22	Y
	41	J10- 4	2	Test I/O	22	W-BK
	42					
	43 44	12V- 1	1	+12V	22	R
	45 46	0V- 2	1	0V	20	BK
	47 48	20V- 2	1	-20V	22	S
	49	85V- 9	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

J9

POWER SWITCHOVER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	Ch. Gnd.		Chassis Ground		
	2					
	3					
	4 5	J16-44	1	+12V from P.S. "A"	20	R
	6 7	J17-44	1	+12V from P.S. "B"	20	R
	8					
	9	J11-35	1	-20V (A) to Pwr. Ctrl.	22	S
	10	J16-48	1	-20V from P.S. "A"	20	S
	11	J16-47	1	-20V from P.S. "A"	20	S
	12	J17-47	1	-20V from P.S. "B"	20	S
	13	J17-48	1	-20V from P.S. "B"	20	S
	13 14	J9-29 J17-49	Jumper 1	-85V from P.S. "B"	22	W-BK
	15	J11-49	1	-85V (B) to Pwr. Ctrl.	22	W-BK
	16	J16-49	1	-85V from P.S. "A"	22	W-BK
	17	J11-36	1	-85V (A) to Pwr. Ctrl.	22	W-BK
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

DRAWN | DATE APPROVED FOR MFG. | J9
CHECKED | REVISIONS | POWER SWITCHOVER
REVIEWED

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29	J9-13	Jumper			
	29	J11-47	1	-20V(B) to Pwr. Ctrl.	22	S
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38	J10-18	1	AC Common	18*	W
	39	J17-1	1	AC Common	18*	W
	40	J17-4	1	AC Switched	18*	W-S
	41	J10-35	1	AC Switched	18*	W-S
	42					
	43	12V-5	1	+12V to Buss	20	R
	44					
	45	0V-11	1	0V from Buss	20	BK
	46	0V-10	1	0V from Buss	20	BK
	47	20V-7	1	-20V to Buss	20	S
	48	20V-6	1	-20V to Buss	20	S
	49	85V-4	1	-85V to Buss	22	W-BK
	50					

NOTES:
*- #18 Twisted Pair

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 21 OF SHEETS

DRAWN | DATE APPROVED FOR MFG. | J10
CHECKED | REVISIONS | TEST CHASSIS
REVIEWED

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5-41	2	Test I/O Input (1)	22	O
	2	J6-41	2	Test I/O Output (2)	22	BL
	3	J7-41	2	Test I/O Output (3)	22	V
	4	J8-41	2	Test I/O Output (4)	22	W-BK
	5	J5-39	2	Test EOW (1)	22	W-O
	6	J6-39	2	Test EOW (2)	22	W-Y
	7	J7-39	2	Test EOW (3)	22	W-G
	8	J8-39	2	Test EOW (4)	22	W-BL
	9	J5-38	2	Test Data (1)	22	W-V
	10	J6-38	2	Test Data (2)	22	W-S
	11	J7-38	2	Test Data (3)	22	BK
	12	J8-38	2	Test Data (4)	22	BL
	13	J6-40	2	Test Gate #2	22	V
	14	J7-40	2	Test Gate #3	22	O
	15	J8-40	2	Test Gate #4	22	Y
	16					
	17					
	18	J9-38	1	AC Common	18ø	W
	18	L2-1	1	Test Playback Ret.	22*	W
	18	J10-34	Jumper			
	19	L2-2	1	Test Playback Sig.	22*	BR
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:
*- #22 Twisted Pair
ø- #18 Twisted Pair

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 22 OF SHEETS

DRAWN | DATE APPROVED FOR MFG. | J10
CHECKED | REVISIONS (Y) | TEST CHASSIS
REVIEWED

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30	J16-35	1	-20V Unreg. (P.S. "A")	22	W-BR
	31					
	32					
	33					
	34	J10-18	Jumper			
	34	J4-37	1	AC Common	18 ø	W
	35	J9-41	1	AC Switched	18 *	W-S
	36	J4-35	1	AC Switched	18 *	W-S
	37					
1	38	S14-D2	2	Operational Interlock	22	Y
	39	P4-C	2	Op. Interlock Return	22	G
	40					
	41	J17-35	1	-20V Unreg. (P.S."B")	22	W-R
	42					
	43	12V-10	1	+12V from Buss	22	R
	44					
	45	0V-20	1	0V from Buss	20	BK
	46					
	47	20V-1	1	-20V from Buss	22	S
	48					
	49					
	50	Ch. Gnd.		Chassis Ground		

NOTES:
*- #18 Twisted Pair
ø- #18 Twisted Pair

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 23 OF SHEETS

DRAWN | DATE APPROVED FOR MFG. | J11
CHECKED | REVISIONS | POWER CONTROL
REVIEWED

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1					
	2					
	3	TB1-1	1	AC Common to Blower	18*	W
	4	J16-1	1	AC Common	18*	W
	5	F2-2	1	AC Common	18*	W
	6					
	7					
	8					
	9	F1-2	1	AC Fused	18*	W-S
	10					
	11					
	12	J16-5	1	AC Switched	18*	W-S
	13					
	14	TB1-2	1	AC Switched to Blower	18*	W-S
	15					
	16					
	17					
	18	J1-39	1	+250V- (1)	22	W-R
	19	J2-39	1	+250V- (2)	22	W-R
	20	J3-39	1	+250V- (3)	22	W-R
	21	J4-39	1	+250V- (4)	22	W-R
	22	J1-38	1	-250V- (1)	22	Y
	23	J2-38	1	-250V- (2)	22	Y
	24	J3-38	1	-250V- (3)	22	Y
	25	J4-38	1	-250V- (4)	22	Y

NOTES: *- #18 Twisted Pair

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 24 OF SHEETS

Rev. 6/15/61

J11

POWER CONTROL

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34	J16-43	1	+12V (A)	22	R
	35	J9- 9	1	-20V (A)	22	S
	36	J9-17	1	-85V (A)	22	W-BK
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	J17-43	1	+12V (B)	22	R
	45	0V-1	1	0V from Buss	20	BK
	46					
	47	J9-29	1	-20V (B)	22	S
	48					
	49	J9-15	1	-85V (B)	22	W-BK
	50					

NOTES:

J12

DUAL 17 BIT S.R. #1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J5 -36	2	C.D. Trigger	22	W-O
	2					
	3					
	4	J 5-12	2	Data Input	22	W-BR
	5					
	6					
	7	J5 -35	2	EOW Input	22	W-R
	8	J5 -6	2	EOW "A"	22	BL
	9	J5 -10	2	EOW "B"	22	W
	10	J5 -4	2	Data "B"	22	Y
	11	J5 -8	2	Data "A"	22	V
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J 14

DUAL 17 BIT S.R. #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	12V- 4	1	+12V	22	R
	45--- 46---]	0V- 5	1	0V	20	BK
	47--- 48---]	20V- 5	1	-20V	20	S
	49	85V- 3	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

J 15

DUAL 17 BIT S.R. #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J8 -36	2	C.D. Trigger	22	W-O
	2					
	3					
	4	J8 -12	2	Data Input	22	W-BR
	5					
	6					
	7	J8 -35	2	EOW Input	22	W-R
	8	J8 -6	2	EOW "A"	22	BL
	9	J8 -10	2	EOW "B"	22	W
	10	J8 -4	2	Data "B"	22	Y
	11	J8 -8	2	Data "A"	22	V
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J 13

DUAL 17 BIT S.R. #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	12V- 8	1	+12V	22	R
	45--- 46---	0V- 18	1	0V	20	BK
	47--- 48---	20V- 10	1	-20V	20	S
	49	85V- 7	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

J14

DUAL 17 BIT S.R. #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J7 -36	2	C.D. Trigger	22	W/O
	2					
	3					
	4	J7 -12	2	Data Input	22	W/BR
	5					
	6					
	7	J7 -35	2	EOW Input	22	W/R
	8	J 7-6	2	EOW "A"	22	BL
	9	J 7-10	2	EOW "B"	22	W
	10	J 7-4	2	Data "B"	22	Y
	11	J 7-8	2	Data "A"	22	V
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J 12

DUAL 17 BIT S.R.#1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	12V-6	1	+12V	22	R
	45--- 46---	0V-16	1	0V	20	BK
	47--- 48---	20V-8	1	-20V	20	S
	49	85V-5	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

J 13

DUAL 17 BIT S.R.#2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J6 -36	2	C.D. Trigger	22	W-O
	2					
	3					
	4	J6 -12	2	Data Input	22	W-BR
	5					
	6					
	7	J6 -35	2	EOW Input	22	W-R
	8	J6 -6	2	EOW "A"	22	BL
	9	J6 -10	2	EOW "B"	22	W
	10	J 6-4	2	Data "B"	22	Y
	11	J6 -8	2	Data "A"	22	V
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES:

J 15

DUAL 17 BIT S.R.#4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35					
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43					
	44	12V-2	1	+12V	22	R
	45--- 46---	0V- 3	1	0V	20	BK
	47--- 48---	20V-3	1	-20V	20	S
	49	85V-1	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

J16

POWER SUPPLY (A)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1--- 2---	J11-4 J17-2	1 1	AC Common AC Common	18* 18*	W W
	3					
	4--- 5---	J17-5 J11-12	1 1	AC Switched AC Switched	18* 18*	W-S W-S
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES: *- #18 Twisted Pair

J16
POWER SUPPLY (A)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35	J10-30	1	-20V, Unreg.	22	W-BR
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43	J11-34	1	+12V	22	R
	44	J9-4	1	+12V	20	R
	45	0V-13	1	0V	20	BK
	46	0V-12	1	0V	20	BK
	47	J9-11	1	-20V	20	S
	48	J9-10	1	-20V	20	S
	49	J9-16	1	-85V	22	W-BK
	50	Ch. Gnd		Chassis Ground		

NOTES:

J17
POWER SUPPLY (B)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J9-39	1	AC Common	18*	W
	2	J16-2	1	AC Common	18*	W
	3					
	4	J9-40	1	AC Switched	18*	W-S
	5	J16-4	1	AC Switched	18*	W-S
	6					
	7					
	8					
	9					
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					
	21					
	22					
	23					
	24					
	25					

NOTES: *- #18 Twisted Pair

J17

POWER SUPPLY (B)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	26					
	27					
	28					
	29					
	30					
	31					
	32					
	33					
	34					
	35	J10-41	1	-20V, Unreg.	22	W-R
	36					
	37					
	38					
	39					
	40					
	41					
	42					
	43	J11-44	1	+12V	22	R
	44	J9-7	1	+12V	20	R
	45	0V-9	1	0V	20	BK
	46	0V-8	1	0V	20	BK
	47	J9-12	1	-20V	20	S
	48	J9-13	1	-20V	20	S
	49	J9-14	1	-85V	22	W-BK
	50	Ch. Gnd.		Chassis Ground		

NOTES:

J18

(POWER INPUT CONNECTOR)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S1-1	Jumper	AC "Hot" Input	14	S
	B	S1-2	Jumper	AC Common Input	14	W
	C	Frame	Jumper	Frame Ground	14	BK
	D					
	E					

NOTES: Connector Type:
MS-3102A-18-11P

J19

OUTPUT CONN. (A)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J5-34	2	Data (1)	22	W-BL
	B	J5-13	2	Copy (1)	22	BR
	C	J5-17	2	EOW (1)	22	O
	D	J6-34	2	Data (2)	22	Y
	E	J6-13	2	Copy (2)	22	G
	F	J6-17	2	EOW (2)	22	BL
	G	J7-34	2	Data (3)	22	V
	H	J7-13	2	Copy (3)	22	W-BR
	J	J7-17	2	EOW (3)	22	W-R
	K	J8-34	2	Data (4)	22	W-O
	L	J8-13	2	Copy (4)	22	W-Y
	M	J8-17	2	EOW (4)	22	W-G
	N					
	P					
	R					
	S					
	T					
	U					
	V	0V-1	2	Signal Return	20	BK

NOTES: Connector type:
MS 3102A-22-14S

J20

OUTPUT CONN. (B)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	J5-16	2	Data (1)	22	W-BL
	B	J5-14	2	Copy (1)	22	BR
	C	J5-15	2	EOW (1)	22	O
	D	J6-16	2	Data (2)	22	Y
	E	J6-14	2	Copy (2)	22	G
	F	J6-15	2	EOW (2)	22	BL
	G	J7-16	2	Data (3)	22	V
	H	J7-14	2	Copy (3)	22	W-BR
	J	J7-15	2	EOW (3)	22	W-R
	K	J8-16	2	Data (4)	22	W-O
	L	J8-14	2	Copy (4)	22	W-Y
	M	J8-15	2	EOW (4)	22	W-G
	N					
	P					
	R					
	S					
	T					
	U					
	V	0V-20	2	Signal Return	20	BK

NOTES: Connector Type:
MS 3102A-22-14S

DRAWN
CHECKED
REVIEWED

DATE APPROVED FOR MFG.

REVISIONS

DP1

DUMMY PLUG #1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S11-A3	2	Recorder #1 Output	*	
	B					
	C					
	D	S11-B3	2	Recorder #1 Return	*	
	E					

NOTES: Connector Type:
MS-3102A-14S-5P
*RG-174/U Coax

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST

A 75WL1A

SHEET 41 OF SHEETS

DRAWN
CHECKED
REVIEWED

DATE APPROVED FOR MFG.

REVISIONS

DP2

DUMMY PLUG #2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S12-A3	2	Recorder #2 Output	*	
	B					
	C					
	D	S12-B3	2	Recorder #2 Return	*	
	E					

NOTES: Connector Type:
MS-3102A-14S-5P
*RG-174/U Coax

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST

A 75WL1A

SHEET 42 OF SHEETS

Rev. 6/15/61

DRAWN	DATE APPROVED FOR MFG.	4/1	DP3
CHECKED			
REVIEWED	REVISIONS 1		DUMMY PLUG #3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S13-A3	2	Recorder #3 Output	*	
	B					
	C					
	D	S13-B3	2	Recorder #3 Return	*	
	E					

NOTES: Connector Type:
MS-3102A-14S-5P
*RG-174/U Coax

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 43 OF SHEETS

DRAWN	DATE APPROVED FOR MFG.	4/1	DP4
CHECKED			
REVIEWED	REVISIONS 1		DUMMY PLUG #4

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S14-A3	2	Recorder #4 Output	*	
	B					
	C					
	D	S14-B3	2	Recorder #4 Return	*	
	E					

NOTES: Connector Type:
MS-3102A-14S-5P
*RG-174/U Coax

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 44 OF SHEETS

Rev. 6/15/61

DRAWN | DATE APPROVED FOR MFG. | P1

CHECKED

REVIEWED | REVISIONS 1 | DATA LINE #1 INPUT CONN.

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
1	A	S11-A1	2	Data Line #1	*	
1	B	S11-D1	2	Operational Interlock	22	Y
	C	P2-B	2	Interlock Wiring	22	Y
1	D	S11-B1	2	Data Line #1 Ret.	*	
	E	Fr. Gnd.		Frame Ground		

NOTES: *RG-174/U Coax

Connector type: MS-3102A-14S-5P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 45 OF SHEETS

DRAWN | DATE APPROVED FOR MFG. | P2

CHECKED

REVIEWED | REVISIONS 0 | DATA LINE #2, INPUT CONN.

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S12-A1	2	Data Line #2	*	
	B	P1-C	2	Interlock Wiring	22	Y
	C	P3-B	2	Interlock Wiring	22	Y
	D	S12-B1	2	Data Line #2 Ret.	*	
	E	Fr.Gnd.		Frame Ground		

NOTES: *RG-174/U Coax

Connector Type:
MS-3102A-14S-5P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA

WIRE LIST | A 75WL1A | SHEET 46 OF SHEETS

Rev. 6/15/61

DRAWN | DATE APPROVED FOR MFG. | P3
CHECKED | REVISIONS (1) | DATA LINE #3 INPUT CONN.
REVIEWED

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S13-A1	2	Data Line #3	*	
	B	P2-C	2	Interlock Wiring	22	Y
	C	P4-B	2	Interlock Wiring	22	Y
	D	S13-B1	2	Data Line #3 Ret.	*	
	E	Fr.Gnd		Frame Ground		

NOTES: *RG-174/U Coax
Connector Type: MS-3102A-14S-5P

MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 47 OF SHEETS

DRAWN | DATE APPROVED FOR MFG. | P4
CHECKED | REVISIONS (1) | DATA LINE #4 INPUT CONN.
REVIEWED

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	A	S14-A1	2	Data Line #4	*	
	B	P3-C	2	Interlock Wiring	22	Y
	C	J10-39	2	Op. Interlock Return	22	G
	D	S14-B1	2	Data Line #4 Return	*	
	E	Fr. Gnd.		Frame Ground		

NOTES: *RG-174/U Coax
Connector Type: MS-3102A-14S-5P

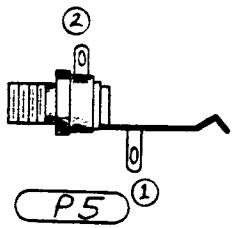
MILGO ELECTRONIC CORPORATION
MIAMI 47, FLORIDA
WIRE LIST | A 75WL1A | SHEET 48 OF SHEETS

Rev. 6/15/61

P5

RECORDING OUTPUT CONN.#1

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J1-49	2	Output to Recorder	#	
	2	J1-46	2	Recorder Return	22	BK



NOTES:
#- RG-174/U Coax
Ground Coax Shield at only one end.

P6

RECORDING OUTPUT CONN.#2

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J2-49	2	Output to Recorder	#	
	2	J2-46	2	Recorder Return	22	BK

P6
(SEE P5)

NOTES:
#- RG-174/U Coax
Ground coax shield at only one end.

P7

RECORDING OUTPUT CONN.#3

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J3-49	2	Output to Recorder	#	
	2	J3-46	2	Recorder Return	22	BK

P7
(SEE P5)

NOTES: #- RG-174/U Coax
Ground Coax Shield at only one end.

P8

RECORDING OUTPUT CONN.#4

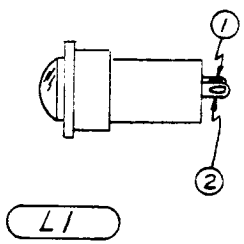
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J4-49	2	Output to Recorder	#	
	2	J4-46	2	Recorder Return	22	BK

P8
(SEE P5)

NOTES: #- RG-174/U Coax
Ground Coax Shield at only one end.

L1
(POWER AVAILABLE LAMP)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	F1-2	1	AC "Hot" Input	20	W-S
	2	F2-2	1	AC Common	20	W

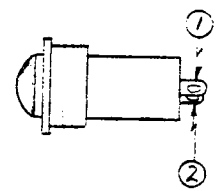


L1

NOTES: Use Insulating Sleeving

L2
(TEST-PLAYBACK LAMP)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J10-18	1	Test Playback Return	22*	W
	2	J10-19	1	Test Playback Sig.	22*	BR



L2

NOTES: *-#22 Twisted Pair

-85V BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J15-49	1	-85V to S.R. (4)	22	W-BK
	2	J7-49	1	-85V to Control (3)	22	W-BK
	3	J14-49	1	-85V to S.R. (3)	22	W-BK
	4	J9-49	1	-85V to SWOVR.	22	W-BK
	5	J12-49	1	-85V to S.R. (1)	22	W-BK
	6	J5-49	1	-85V to Control (1)	22	W-BK
	7	J13-49	1	-85V to S.R. (2)	22	W-BK
	8	J6-49	1	-85V to Control (2)	22	W-BK
	9	J8-49	1	-85V to Control (4)	22	W-BK
	10					
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

-20V BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J10-47	1	-20V to Test Chassis	22	S
	2	J8-47	1	-20V to Control (4)	22	S
	3	J15-47	1	-20V to S.R. (4)	20	S
	4	J7-47	1	-20V to Control (3)	22	S
	5	J14-47	1	-20V to S.R. (3)	20	S
	6	J9-48	1	-20V to SWOVR.	20	S
	7	J9-47	1	-20V to SWOVR.	20	S
	8	J12-47	1	-20V to S.R. (1)	20	S
	9	J5-47	1	-20V to Control (1)	22	S
	10	J13-47	1	-20V to S.R. (2)	20	S
	11	J6-47	1	-20V to Control (2)	22	S
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

0V BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J11-45	1	0V to PWR. CTRL.	20	BK
	1	J19-V	2	Signal Return	20	BK
	2	J8-45	1	0V to Control (4)	20	BK
	3	J15-45	1	0V to S.R. (4)	20	BK
	4	J7-45	1	0V to Control (3)	20	BK
	5	J14-45	1	0V to S.R. (3)	20	BK
	6	J4-45	1	0V to D.L.A. (4)	20	BK
	7	J3-45	1	0V to D.L.A. (3)	20	BK
	8	J17-46	1	0V to P.S. (B)	20	BK
	9	J17-45	1	0V to P.S. (B)	20	BK
	10	J9-46	1	0V to PWR. SWOVR	20	BK
	11	J9-45	1	0V to PWR. SWOVR.	20	BK
	12	J16-46	1	0V to P.S. (A)	20	BK
	13	J16-45	1	0V to P.S. (A)	20	BK
	14	J1-45	1	0V to D.L.A. (1)	20	BK
	15	J2-45	1	0V to D.L.A. (2)	20	BK
	16	J12-45	1	0V to S.R. (1)	20	BK
	17	J5-45	1	0V to Control (1)	20	BK
	18	J13-45	1	0V to S.R. (2)	20	BK
	19	J6-45	1	0V to Control (2)	20	BK
	20	J10-45	1	0V to Test Chassis	20	BK
	20	J20-V	2	Signal Return	20	BK

NOTES:

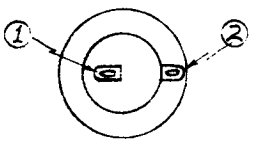
+12V BUSS

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J8-43	1	+12V to Control (4)	22	R
	2	J15-44	1	+12V to S.R. (4)	22	R
	3	J7-43	1	+12V to Control (3)	22	R
	4	J14-44	1	+12V to S.R. (3)	22	R
	5	J9-43	1	+12V to PWR.SWOVR.	20	R
	6	J12-44	1	+12V to S.R. (1)	22	R
	7	J5-43	1	+12V to Control (1)	22	R
	8	J13-44	1	+12V to S.R. (2)	22	R
	9	J6-43	1	+12V to Control (2)	22	R
	10	J10-43	1	+12V to Test Chassis	22	R
	11					
	12					
	13					
	14					
	15					
	16					
	17					
	18					
	19					
	20					

NOTES:

F1 and F2
LINE FUSES

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	F1-1	S1-3	Jumper	AC "Hot"	14	S
	F1-2	J11-9	1	AC "Hot"	18	W-S
	F1-2	L1-1	1	AC Switched	20	W-S
	F2-1	S1-4	Jumper	AC Common	14	W
	F2-2	J11-5	1	AC Common	18	W
	F2-2	L1-2	1	AC Common	20	W

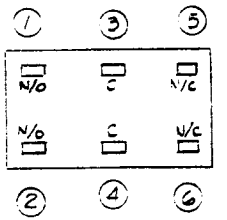


F1, F2

NOTES:

S1
(LINE SWITCH)

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J18-A	Jumper	AC Hot	14	S
	2	J18-B		AC Common	14	W
	3	F1-1		AC Hot	14	S
	4	F2-1		AC Common	14	W
	5					
	6					

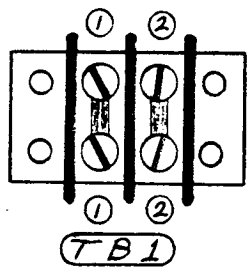


S1

NOTES: Use Insulating Sleeving

TB1

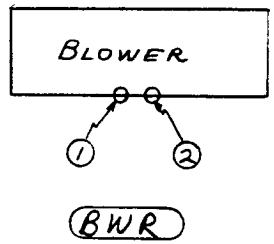
WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	J11-3	1	AC Common	18*	W
	1	BWR-1		AC Common to Blower	18	W
	2	J11-14	1	AC Switched	18*	S
	2	BWR-2		AC to Blower	18	S



NOTES: *- #18 Twisted Pair to J11

BWR
BLOWER

WIRE NO.	TERMINAL	DESTINATION	CABLE	IDENTIFICATION	WIRE SIZE	COLOR
	1	TB1-1	1	AC Common	18	W
	2	TB1-2	1	AC to Blower	18	S



NOTES:

CHAPTER IX

SCHEMATICS AND DIAGRAMS

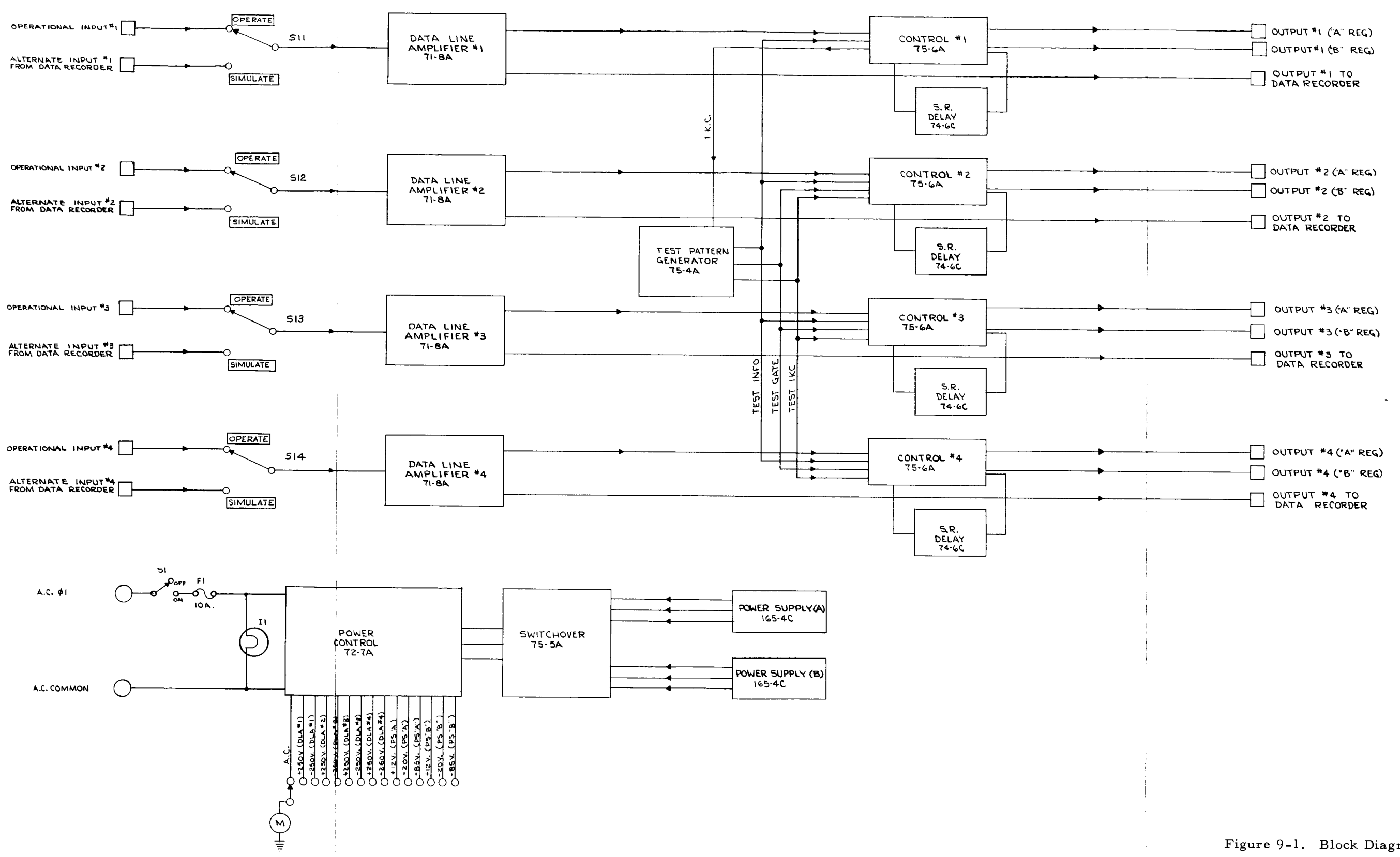


Figure 9-1. Block Diagram
Model 75 Data Receiver
Dwg. #D75B1A, Sheet #1

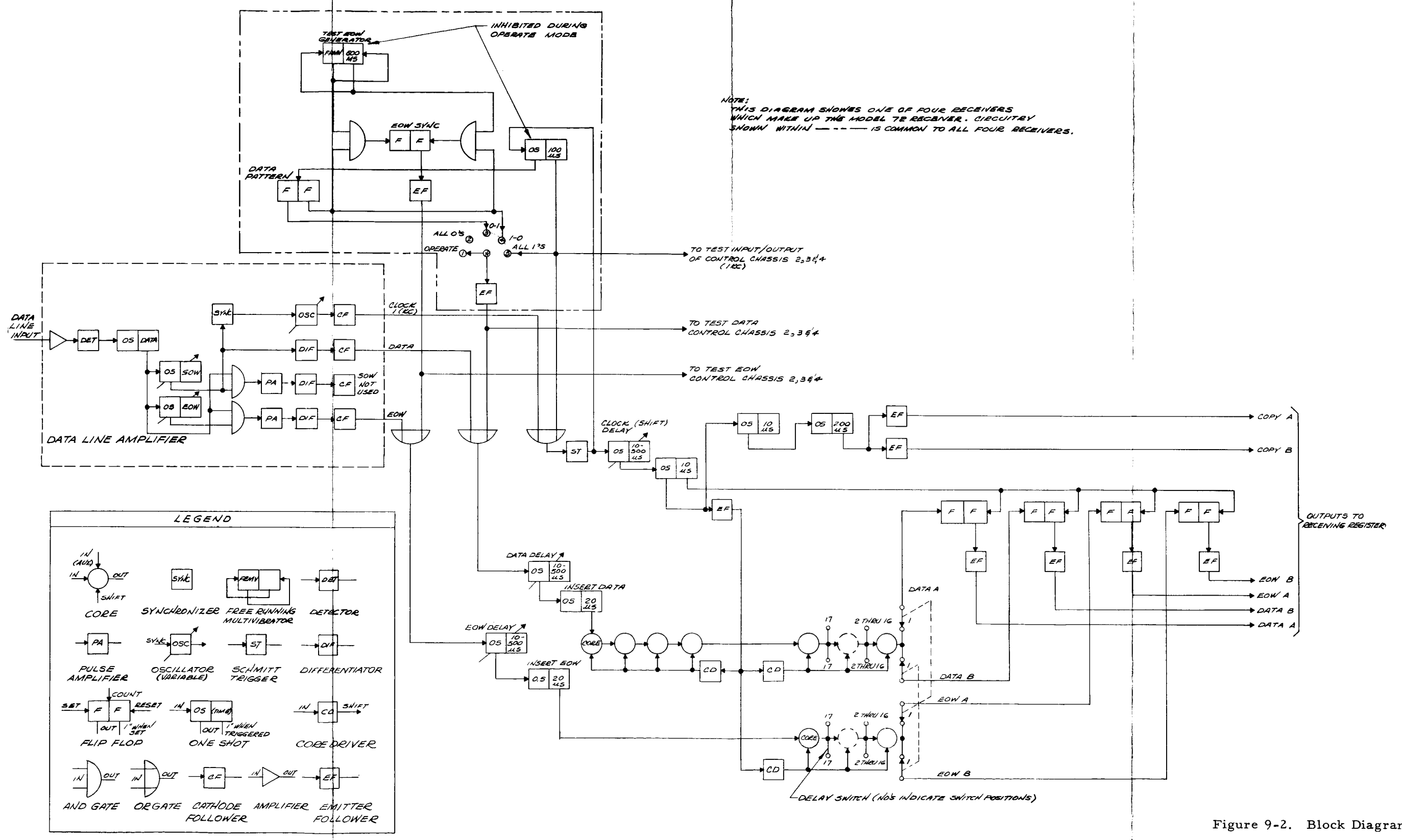


Figure 9-2. Block Diagram
Model 75 Data Receiver
Dwg. #D75B1A, Sheet #2

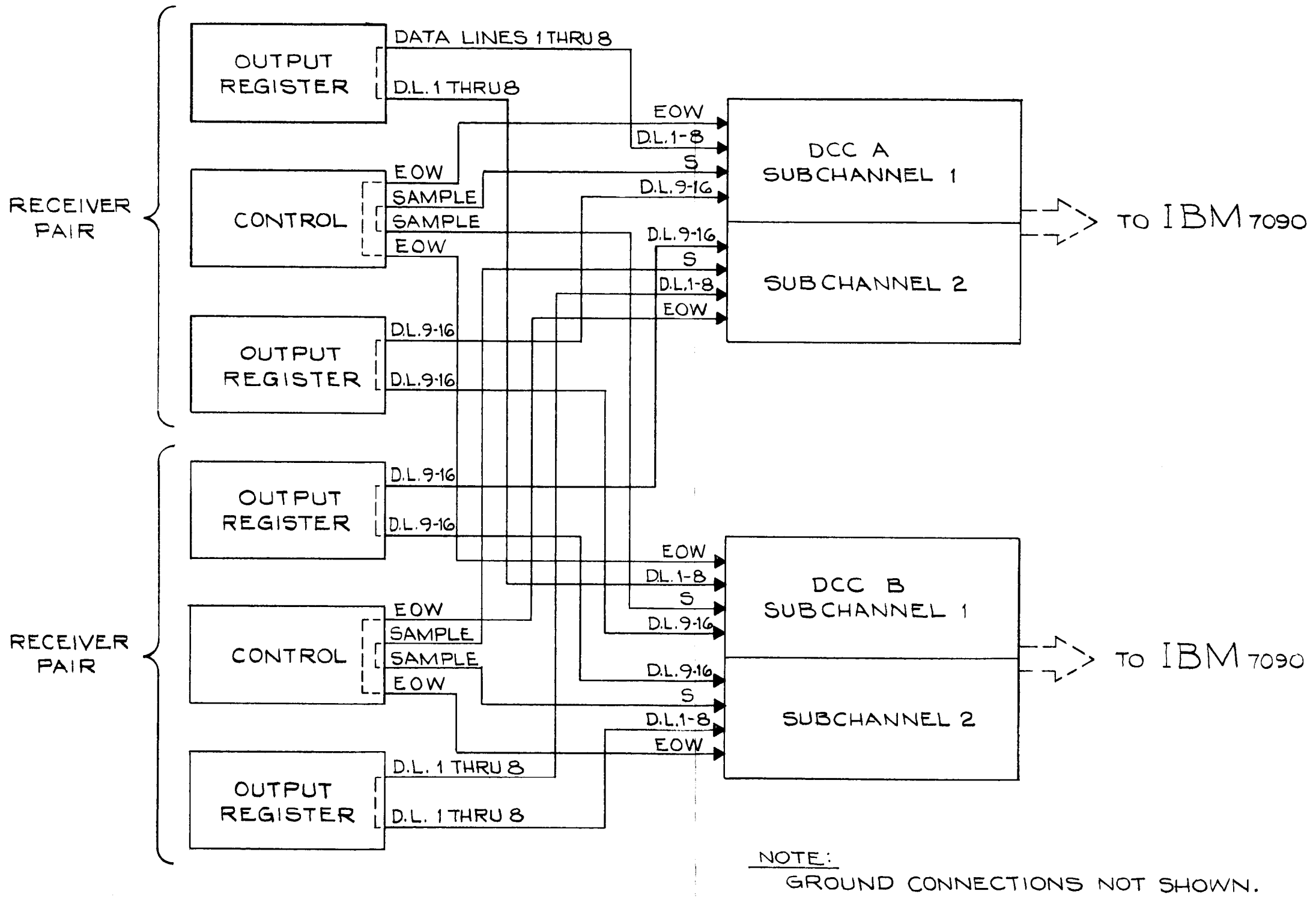
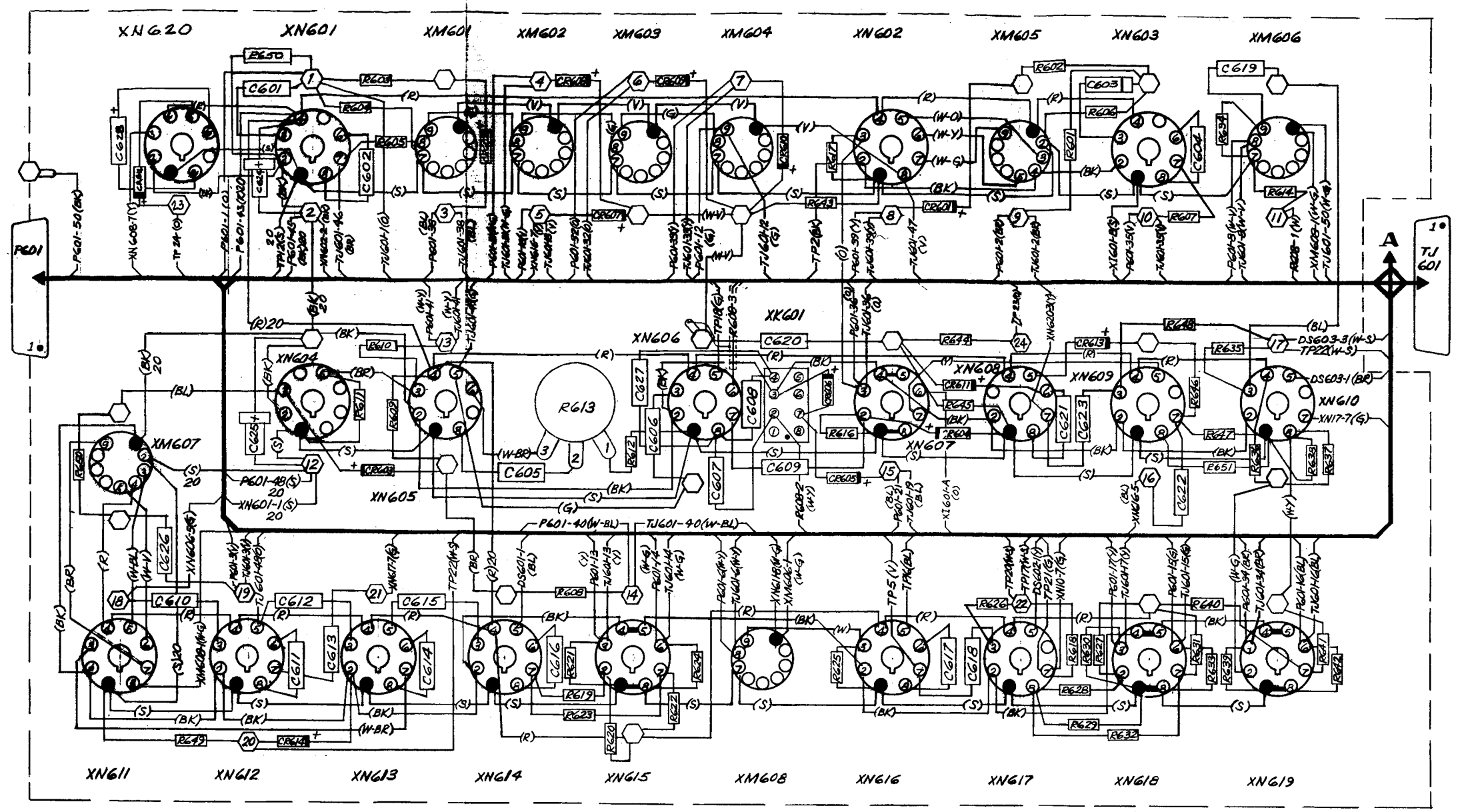
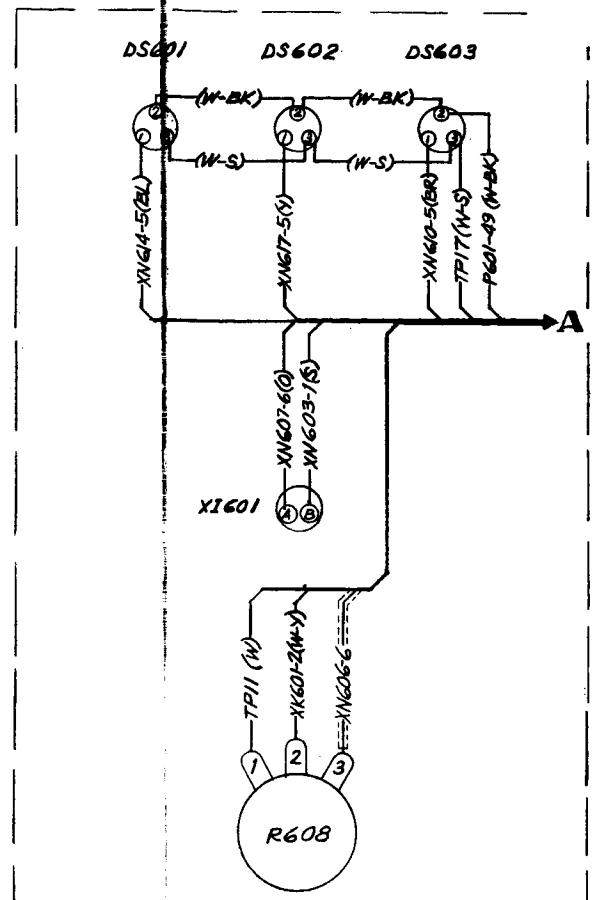


Figure 9-2. Receiver-DCC Connections

Figure 9-4. Schematic
Control Chassis
Dwg. #D75S6B





NOTES:
1. UNLESS OTHERWISE SPECIFIED ALL WIRE TO BE #22 GA.
2. JUMPER PINS ON CONNECTOR AS SHOWN.
3. ALL COAX TO BE RG 174/U

P601

PIN	DESTINATION	FUNCTION	WIRE
1	TP1	DATA FROM DLA	O
2	TP9	FDW FROM DLA	BR
3	TP19	I.K.C. FROM DLA	V
4			
5			
6	XM606R-A	FDW "A" FROM 12 BIT S.R.	W-Y
7			
8	XM606-R	DATA "A" FROM 12 BIT S.R.	W-V
9			
10			
11			
12	XM604-9	DATA TO 12 BIT S.R.	G
13	XN615-9	COPY TO "A" REG.	Y
14	XN615-6	COPY TO "B" REG.	W-G
15	XN618-6	FDW TO "B" REG.	G
16	XN619-6	DATA TO "A" REG.	BL
17	XN618-3	FDW TO "A" REG.	V
18	TP8	FDW TO (A) CONTROL	V
19			
20			
21	TP15		BL
22			
23			
24			
25			

PIN	DESTINATION	FUNCTION	WIRE
26			
27			
28			
29			
30			
31	TP4	FDW FROM (B) CONTROL	W-G
32	TP6		O
33	TP7		Y
34	XN619-3	DATA TO "B" REG.	BR
35	TP10	FDW TO 12 BIT S.R.	V
36	XN607-3	SHIFT TO 12 BIT S.R.	O
37			
38	TP3	TEST DATA	BL
39	TP8	TEST FDW	Y
40	TP14	TEST GATE	W-BL
41	TP13	TEST INPUT/OUTPUT	W-Y
42			
43	XN601-6	+12 V	(R)20
44		+12 V	
45	TP2	0 V	(BK)20
46		0 V	
47		-20 V	
48	TP12	-20 V	(S)20
49	XN601-2	-28 V	W-BK
50	GND LUG	CHASSIS GND	BK

SEE NOTE #2

SEE NOTE #2

TJ601

PIN	DESTINATION	FUNCTION	WIRE
1	TP1	DATA FROM DLA	O
2	TP9	FDW FROM DLA	BR
3	TP19	I.K.C. FROM DLA	V
4			
5			
6	XM606R-B	FDW "A" FROM 12 BIT S.R.	W-Y
7			
8	XM606-R	DATA "A" FROM 12 BIT S.R.	W-V
9			
10			
11			
12	XM604-9	DATA TO 12 BIT S.R.	G
13	XN615-3	COPY TO "A" REG.	Y
14	XN615-6	COPY TO "B" REG.	W-G
15	XN618-6	FDW TO "A" REG.	G
16	XN619-6	DATA TO "A" REG.	BL
17	XN618-3	FDW TO "A" REG.	V
18	TP8	FDW TO (A) CONTROL	V
19	TP15		BL
20			
21			
22			
23			
24			
25			

PIN	DESTINATION	FUNCTION	WIRE
26			
27			
28			
29			
30			
31	TP4	FDW FROM (B) CONTROL	W-G
32	TP6		O
33	TP7		Y
34	XN619-3	DATA TO "B" REG.	BR
35	TP10	FDW TO 12 BIT S.R.	V
36	XN607-3	SHIFT TO 12 BIT S.R.	O
37			
38	TP3	TEST DATA	BL
39	TP8	TEST FDW	Y
40	TP14	TEST GATE	W-BL
41	TP13	TEST INPUT/OUTPUT	W-Y
42			
43			
44			
45			
46	XN601-7		BR
47	XN602-8	SHIFT	V
48	XN612-6		O
49	XN605-5		G
50	XM606-L	SHIFT	W-G

Figure 9-5. Wiring Diagram
Control Chassis
Dwg. #D75W6B

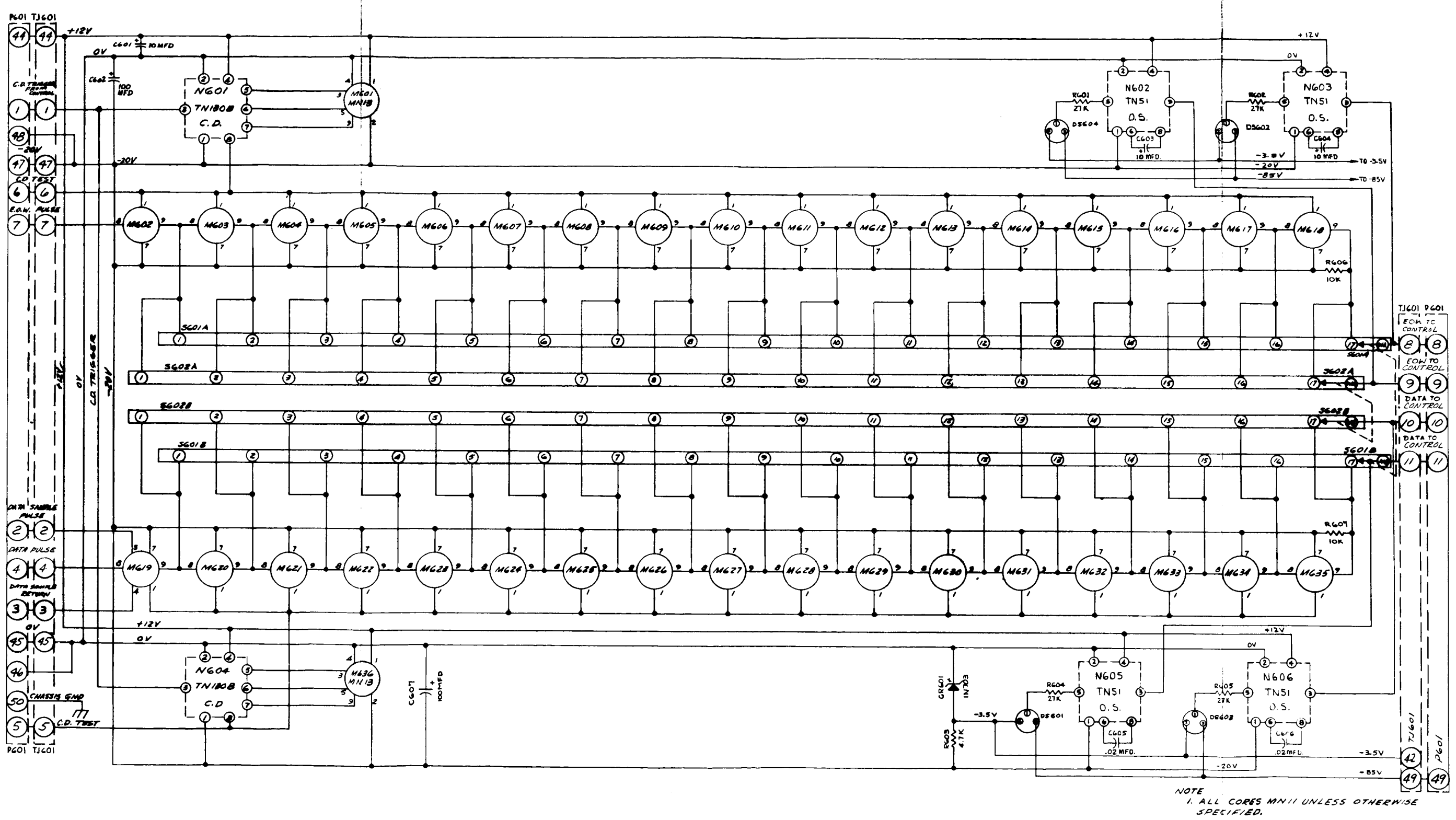


Figure 9-6. Schematic,
Dual 17 Bit Shift Register,
Dwg. #D74S6C

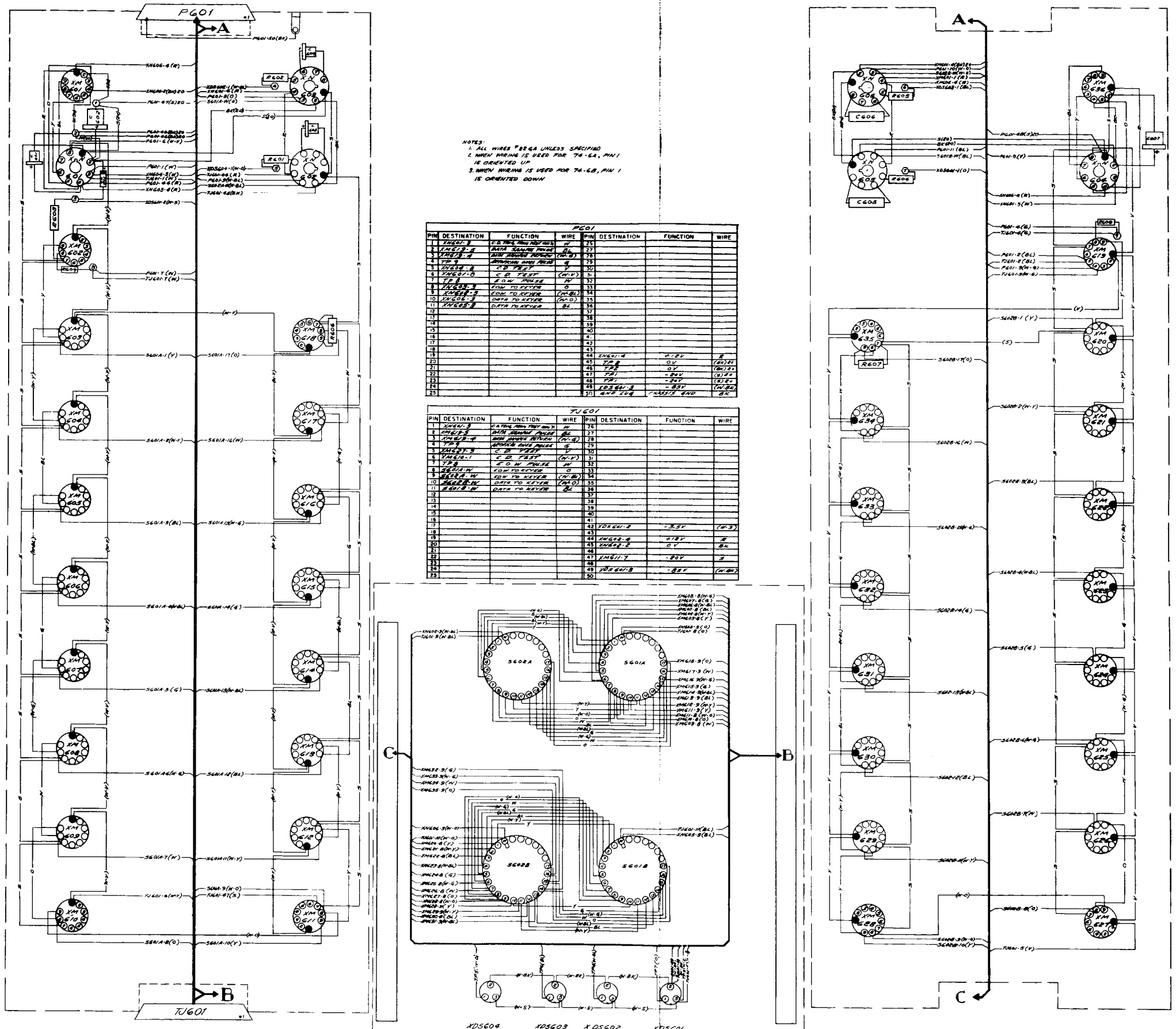
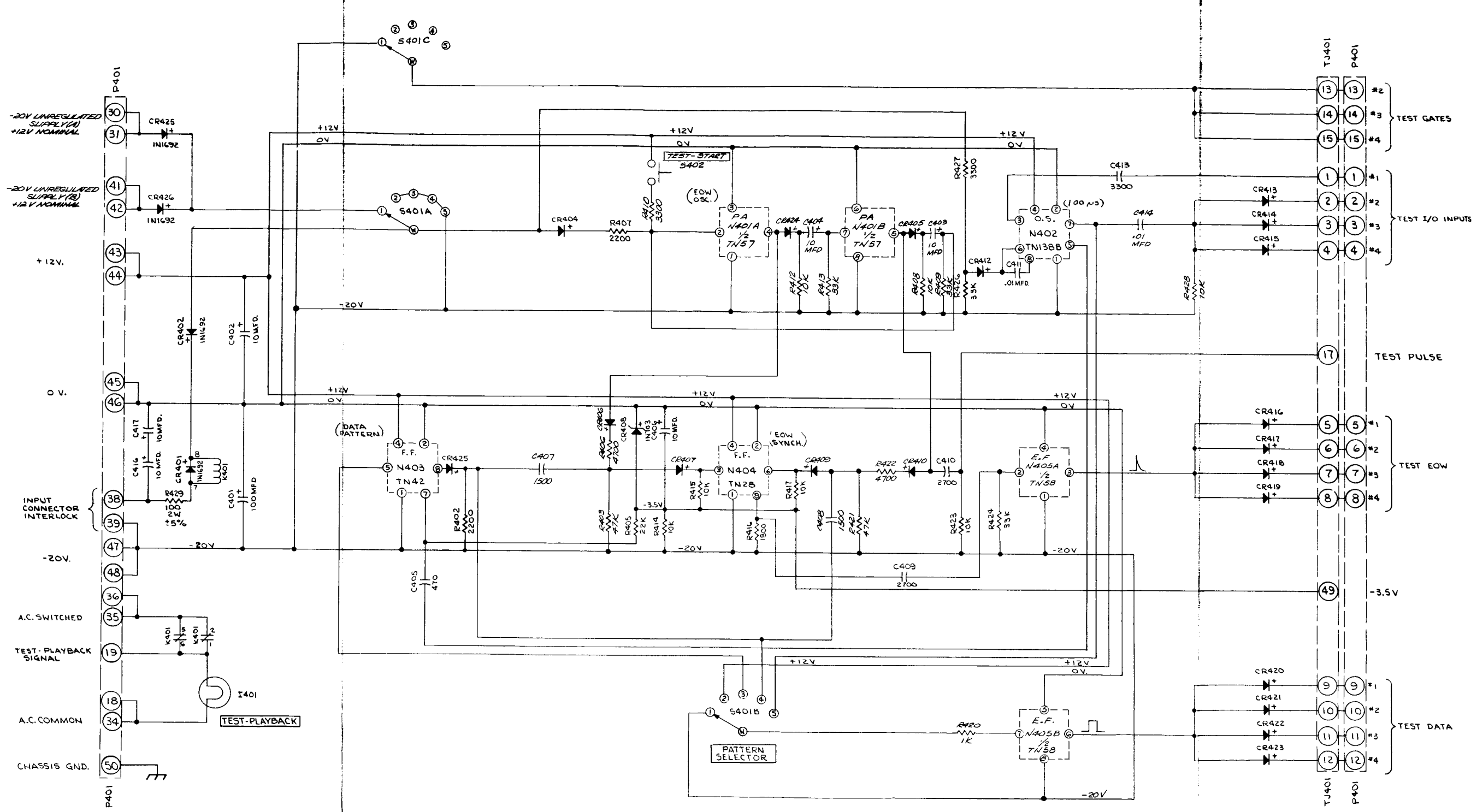


Figure 9-7. Wiring Diagram, Dual 17 Bit Shift Register, Dwg. #E74W6A

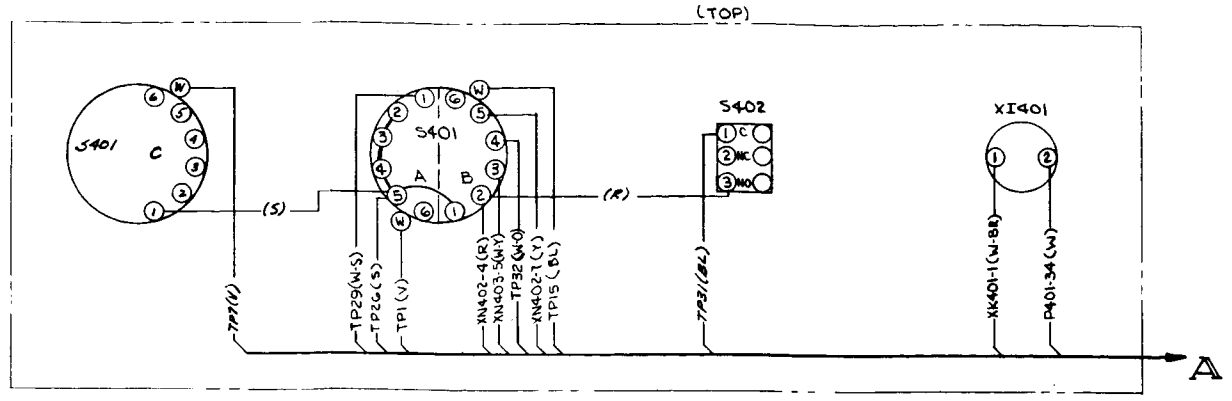


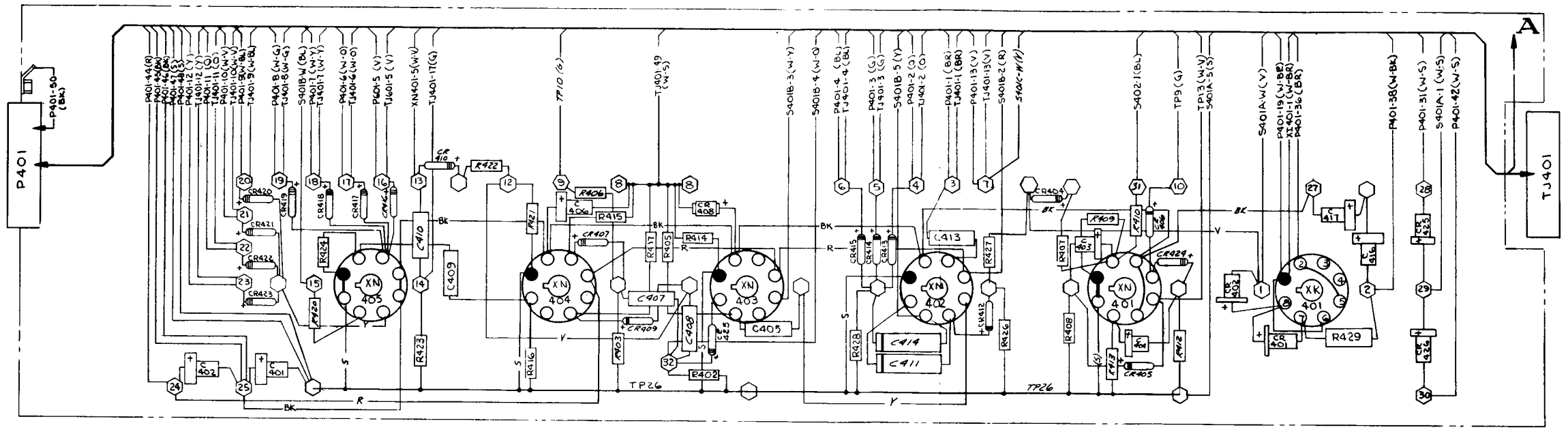
PATTERN SWITCH - S401	
POSITION	FUNCTION
1	OPERATE
2	ALL 0's
3	01
4	10
5	ALL 1's

NOTES:
1. ALL DIODES TO BE CTP503 OR T12G UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS TO BE 1/2 W. ±10% UNLESS OTHERWISE SPECIFIED.

UNLESS OTHERWISE SPECIFIED.
1. Capacitance is in mmf.
2. Resistance is in ohms.

Figure 9-8. Schematic, Test Pattern Generator, Dwg. #D75S4A





TJ401			
PIN	DESTINATION	FUNCTION	WIRE
1	TP3	#1 TEST I/O INPUT	BR
2	TP4	#2	O
3	TP5	#3	G
4	TP6	#4	BL
5	TP16	#1 TEST EOW	V
6	TP17	#2	W-O
7	TP18	#3	W-Y
8	TP19	#4	W-G
9	TP20	#1 TEST DATA	W-BL
10	TP21	#2	W-V
11	TP22	#3	O
12	TP23	#4	Y
13	TP7	#2 TEST GATE	V
14		#3	
15		#4	
16		TEST PULSE	G
17	TP14		
18			
19			
20			
21			
22			
23			
24			
25			
49	TP8	-3.9V	W-S

P401							
PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1	TP3	#1 TEST I/O INPUT	BR	26			
2	TP4	#2	O	27			
3	TP5	#3	G	28			
4	TP6	#4	BL	29			
5	TP16	#1 TEST EOW	V	30		-20V. UNREG.(A)	
6	TP17	#2	W-O	31	TP28	-20V. UNREG. (A)	W-S
7	TP18	#3	W-Y	32			
8	TP19	#4	W-G	33			
9	TP20	#1 TEST DATA	W-BL	34	XI401-2	A.C. COMMON	W
10	TP21	#2	W-V	35		A.C. SWITCHED	BR
11	TP22	#3	O	36	XK401-2	A.C. SWITCHED	BR
12	TP23	#4	Y	37			
13	TP7	#2 TEST GATE	V	38	TP2	INTERLOCK	W-BK
14		#3		39		INTERLOCK	
15		#4		40			
16				41		-20V. UNREG. (B)	
17				42	TP30	-20V. UNREG. (B)	W-S
18		A.C. COMMON		43		+12V.	
19	XK401-1	TEST-PLAYBACK SIG.	W-BR	44	TP24	+12V.	R
20				45	TP25	0V.	BK
21				46	TP25	0V.	BK
22				47	TP26	-20V.	S
23				48	TP26	-20V.	S
24				49			
25				50	GND. LUG	CHASSIS GND.	BK

NOTES:

1. ALL WIRE TO BE #22 GA. UNLESS OTHERWISE SPECIFIED.
2. JUMPER PINS 13,14,15 & 18,34 & 35,36 & 39,47,48 & 41,42 & 43,44 & 30,31 & 45,46 AS SHOWN ON P401 TABLE.
3. JUMPER PINS 13,14,15 AS SHOWN ON TJ401 TABLE

Figure 9-9. Wiring Diagram, Test Pattern Generator, Dwg. #D75W4A

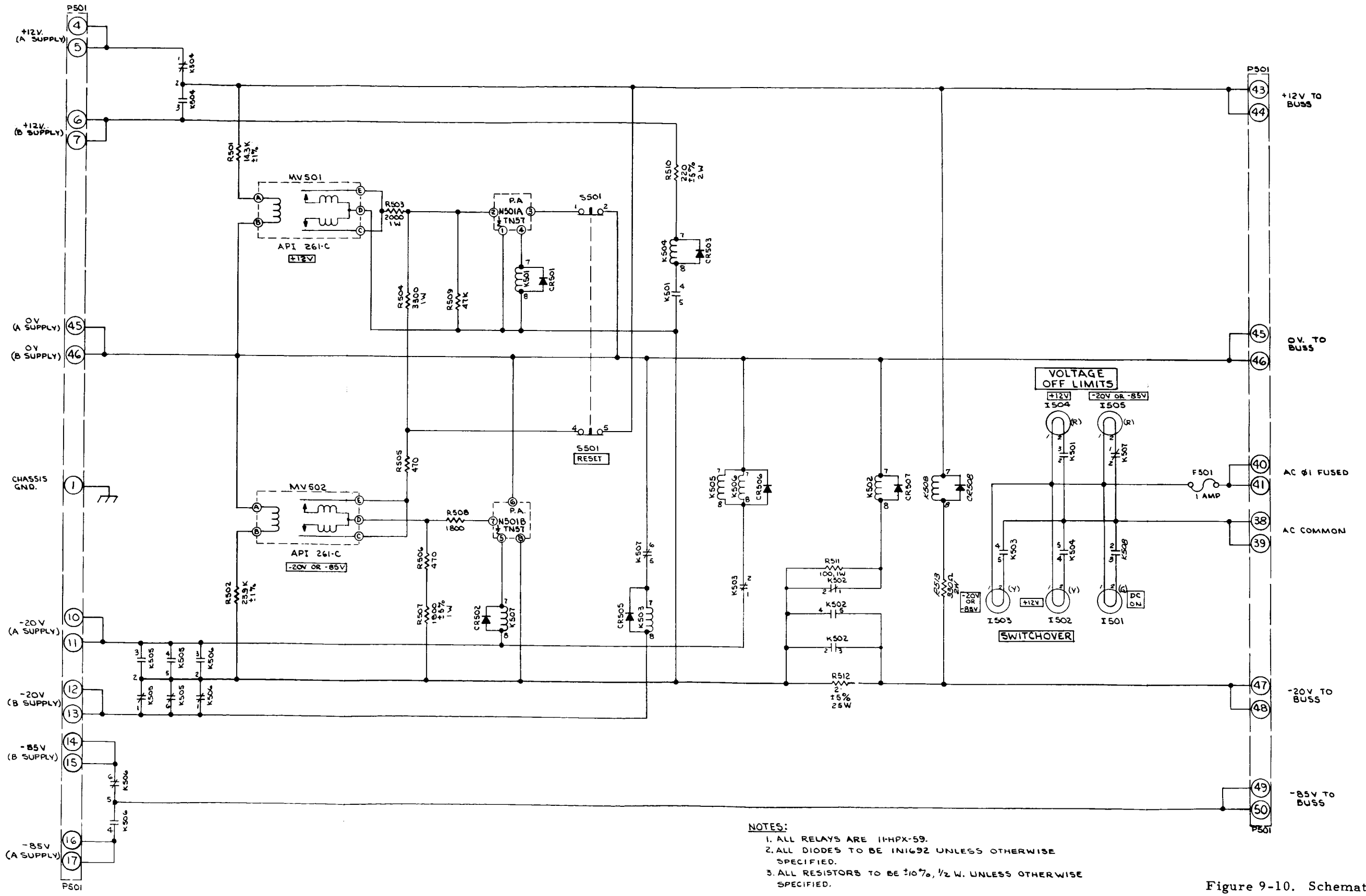
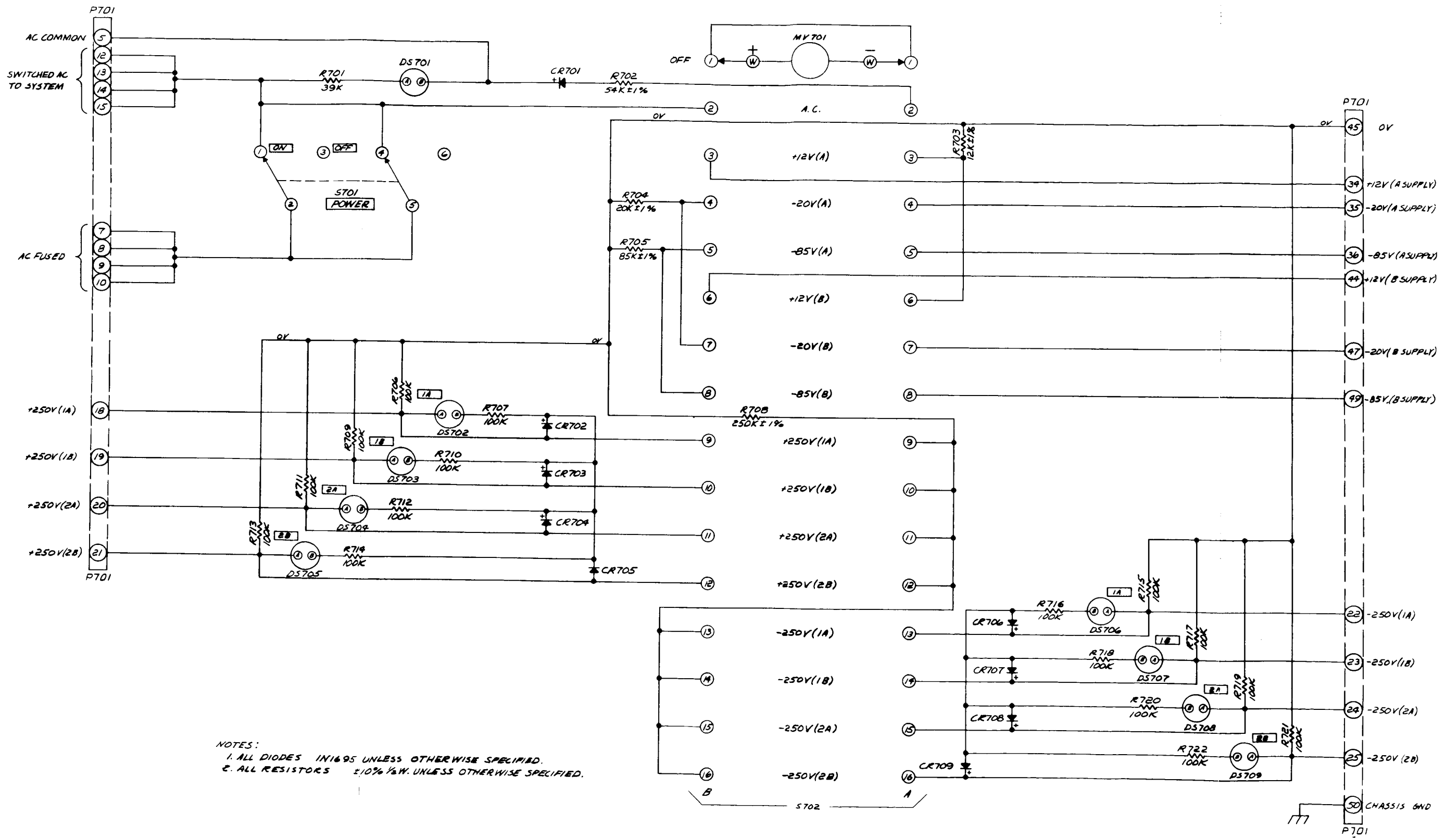
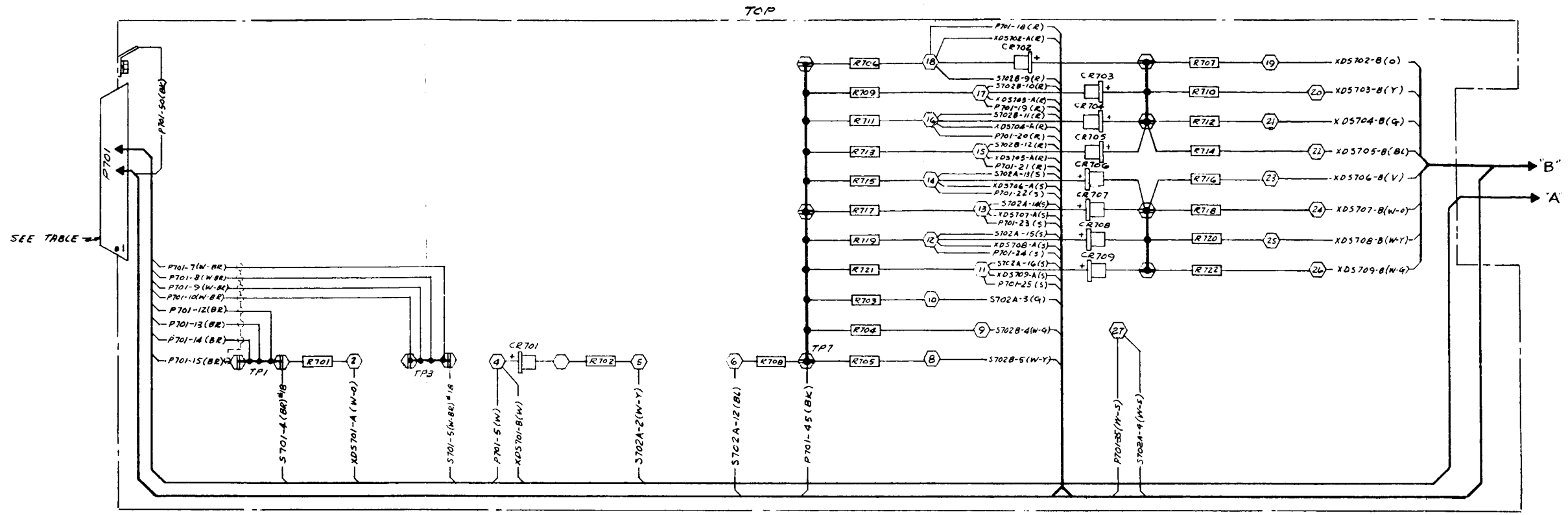


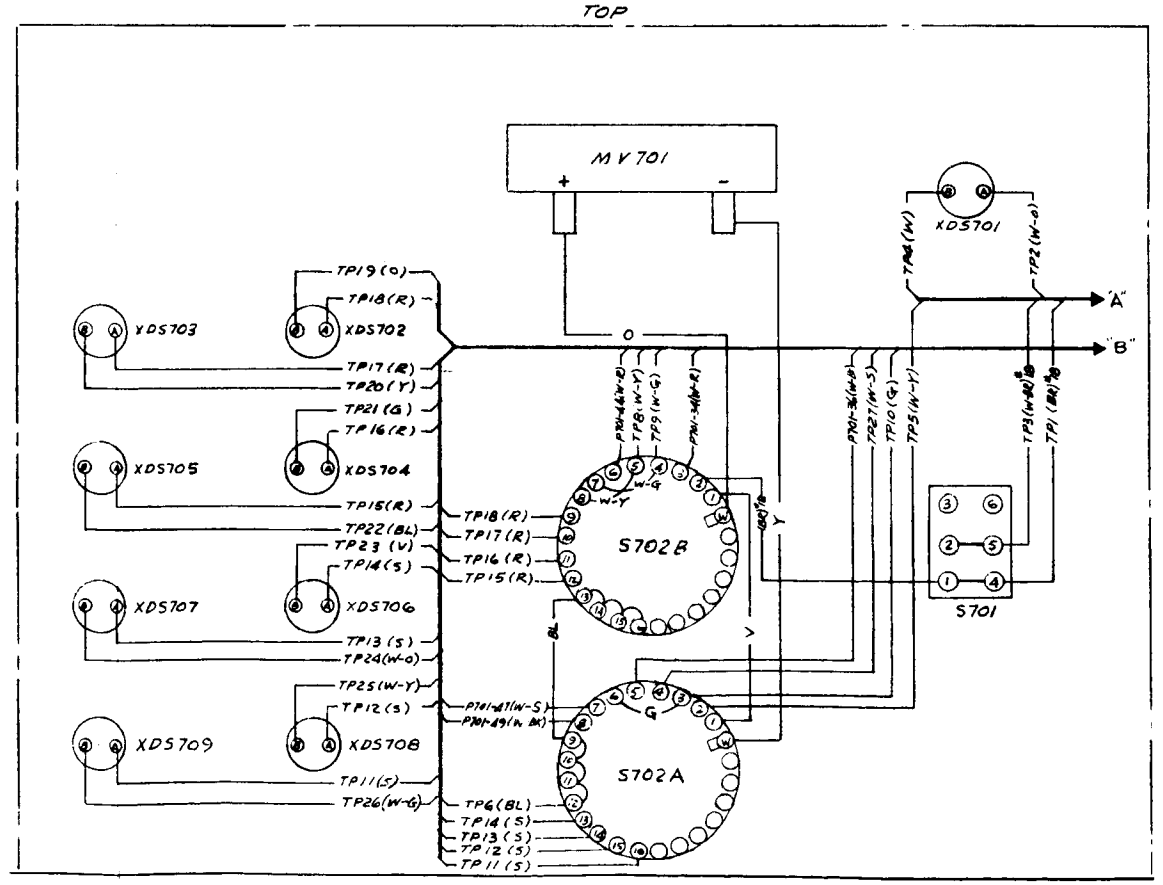
Figure 9-10. Schematic, Switchover Chassis, Dwg. #D75S5A



NOTES:
1. ALL DIODES IN1695 UNLESS OTHERWISE SPECIFIED.
2. ALL RESISTORS ±10% ½W. UNLESS OTHERWISE SPECIFIED.

Figure 9-12. Schematic, Power Control Chassis, D72S7B





PIN	DESTINATION	FUNCTION	WIRE	PIN	DESTINATION	FUNCTION	WIRE
1				26			
2				27			
3				28			
4				29			
5	TP4	AC COMMON	W	30			
6				31			
7	TP3	AC FUSED	W-BK	32			
8	↓	↓	↓	33			
9	↓	↓	↓	34	S702B-3	+18V (A SUPPLY)	W-R
10	TP3	AC FUSED	W-BK	35	TP22	-26V (A SUPPLY)	W-S
11	TP1	SWITCHED AC TO SYSTEM	BR	36	S702A-5	-85V (A SUPPLY)	W-BK
12	↓	↓	↓	37			
13	↓	↓	↓	38			
14	↓	↓	↓	39			
15	TP1	SWITCHED AC TO SYSTEM	BR	40			
16				41			
17				42			
18	TP18	+250V (A)	R	43			
19	TP17	+250V (B)	R	44	S702B-6	+18V (B SUPPLY)	W-R
20	TP16	+250V (BA)	R	45	TP7	0V	BK
21	TP15	+350V (2B)	R	46			
22	TP14	-250V (A)	S	47	S702A-7	-20V (B SUPPLY)	W-S
23	TP13	-250V (B)	S	48			
24	TP12	-250V (BA)	S	49	S702A-8	-85V (B SUPPLY)	W-BK
25	TP11	-250V (2B)	S	50	GND LUG	CHASSIS GND	BK

NOTES:
1. ⟨S-⟩ DENOTES TWISTED LEADS.
2. S702A DECK NEAREST FRONT PANEL.

Figure 9-13. Wiring Diagram, Power Control Chassis, Dwg. #D72W7B

Figure 9-14. Schematic Operate-Simulate Switch Panel Dwg. #7551AA

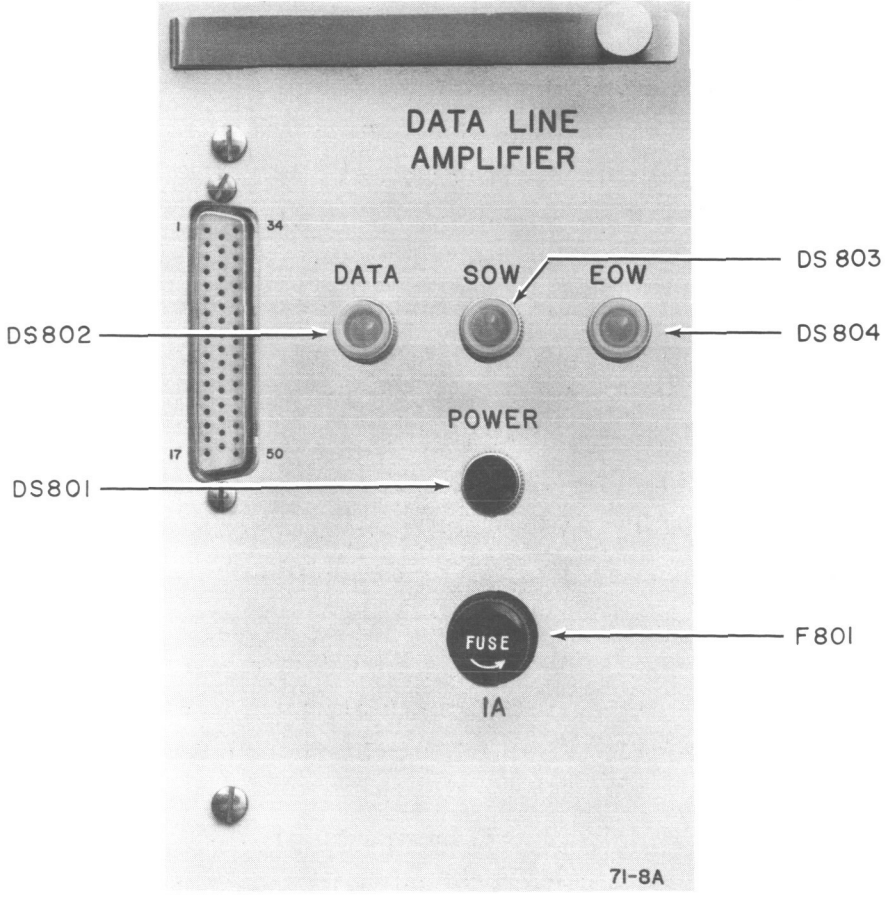
CHAPTER X

APPENDIX

DATA LINE AMPLIFIER
MEC MODEL 71-8 A

1. GENERAL

1-1. The Data Line Amplifier receives data in the form of modulated tone bursts of approximately 2 kc at a 1 kc repetition rate from 3 kc voice channels on balanced or unbalanced communication lines, equalized for 1 kc data bit rate. The tone bursts for data are 0.5 milliseconds. The bursts for Start of Word (SOW) and End of Word (EOW) may vary in length depending on the system in which the Data Line Amplifier is used. In some systems, SOW and/or EOW may not be used. The outputs are a 1 kc sinusoidal waveform which is synchronized to data, and pulse outputs of 10 to 20 volts, depending upon termination, approximately 10 microseconds wide, for data, SOW, and EOW. The pulse outputs are cathode follower outputs and require terminating resistors external to the chassis. The Data Line Amplifier Input-Output Relationships figure shows the relationships of incoming and outgoing data. The unit operates on 115 volts ± 10 vac and has a self contained power supply for generating regulated +250 volts and -250 volts for use within the chassis.



Data Line Amplifier

2. DETAILED DESCRIPTION

2-1. Incoming Signals - Data enters the chassis in the form described in paragraph 1-1, at pins 15 and 17 of P801. The inputs are connected to pins 1 and 2 of the bridging transformer T801, which has a 10,000 ohm input impedance. External resistors must be used to match the communication line impedance, normally 600 ohms. This makes it possible for one or more receiving line amplifiers to be used on a single circuit, if so desired. The signal is then filtered in a band pass filter for noise rejection before entering the first stage of amplification. The incoming signal can be seen unfiltered at TJ801, pin 16. However, at this point, the circuit is loaded with the filter impedance and does not give a true representation. The filtered signal can be seen at TJ801, pin 50. Potentiometer R801 provides level selection of the incoming signal to the amplifier and is nominally set for a signal swing of approximately 0.5 volts peak to peak at pin 2 of R801. The filtered signal is a-c coupled to the control grid, pin 1, of V801. This is a remote cut-off pentode tube with AGC applied as bias to the control grid through R802. The signal at the output, pin 5 of V801, is a-c coupled to the grid (pin 2) of V802A which provides the second stage of amplification. The output of V802A pin 1, drives a phase splitter, V802B at pin 7, which has outputs at pins 8 and 6 which are out of phase; that is, when pin 6 is going positive, pin 8 is going negative and vice versa. An output at the junction of R812 and R882 in the cathode of V802B is provided for purposes of recording the data on tape. Each output of the phase splitter drives one-half of V803, a push-pull amplifying stage with a common cathode resistor, R816. The outputs of V803, pins 1 and 6, drive the detector, composed of diodes CR801, CR802, and related circuitry. The anodes of these diodes are clamped to 0 volts by diode CR803. Potentiometer R822 determines the d-c bias at the cathodes of the detecting diodes, and in this way determines the amount of the negative going a-c component of the signal from V803 which will appear at the grid, pin 2 of V804A. V804A is an amplifier which is biased near full conduction by R883 and CR803 which clamps the grid voltage to 0 volts. Negative going pulses from pin 1 or 6 of V803, which exceed the bias voltage determined by R822, cause diode CR801 or CR802 to conduct, turning off V804A and producing a positive pulse at its output, pin 1. Negative pulses at the diode detector output also conduct through diode CR804, are filtered, and applied to the grid of V801, the first stage of the amplifier, for AGC action. The detected signal at the output of V804A is amplified and inverted by V804B which drives the logic circuitry. The waveforms of the detected signal are shown in the Data Line Amplifier Waveform Figure.

2-2. Logic - The negative going edge of the detected signal triggers the data one-shot, V805, a 450 microsecond one-shot, which in turn produces a positive going pulse at pin 6 triggering the SOW one-shot V806, and the EOW one-shot V807; three conditions are now possible:

a. The incoming signal is a data burst. In this case, the data one-shot V805, completes its time delay in 450 microseconds and triggers off the SOW and EOW one-shots as pin 6 of V805 goes negative.

b. The incoming signal is a SOW burst. In this case, the data one-shot continues to receive negative pulses and does not complete its time delay in 450 microseconds. The SOW one-shot V806, is not triggered off, but completes its time delay at a time determined by R849 (normally 2 milliseconds). The EOW one-shot V807, is triggered off by the data one-shot because the incoming code burst has ended (normally 2.5 milliseconds) before the EOW one-shot could complete its time delay.

c. The incoming signal is an EOW burst. When the data one-shot is held on for that duration, both the SOW and EOW one-shots complete their time delays before the data one-shot can trigger them off. The period of the EOW one-shot is determined by R843 and is normally 4 milliseconds.

2-3. As the SOW one-shot is triggered on for every data code burst, its output at pin 6 is used to drive the data output cathode follower at pin 7 of V808. This reduces loading on the data one-shot. The grid of the data cathode follower is biased at approximately -25 volts. The cathode is normally returned through an external resistor to -20 volts. The cathode follower will now conduct when positive pulses occur at the grid, producing a positive output pulse approximately 10 microseconds wide at the mid-point and 20 volts in amplitude, each time there is an incoming data burst, SOW burst, or EOW burst. A neon indicator, DS802, connected to the plate, pin 1, of the data one-shot V805, indicates when data is triggering the data one-shot. This data indicator glows faintly during data absence, but increases in intensity when data is present.

2-4. SOW is recognized by the fact that the SOW one-shot has completed its time delay before the data one-shot has returned to its quiescent state (this will occur for both incoming SOW and EOW). When the incoming signal consists of data bursts, and the SOW one-shot is being triggered on by the leading edge of the data one-shot, and off by the trailing edge, the two one-shot waveforms have basically the same width. The negative going pulse from the data one-shot, pin 1 of V805, is connected to the plate of CR806, which is one leg of a diode gate for detecting SOW. The positive going pulse from the SOW one-shot, pin 6 of V806, is connected to the plate of CR805, which is the remaining leg of the gate for recognizing SOW. When the two pulses to CR805 and CR806 have the same width, the junction of the two diodes is maintained positive, keeping the grid of V810B, pin 7, at a voltage which will retain that half of the tube in full conduction, as diode CR811 clamps the voltage to the grid at 0 volts. Capacitors C817 and C825 filter spikes that occur as a result of slight discrepancies of switching times. When an SOW burst occurs, the SOW one-shot completes its time delay, but the data one-shot is still on. This situation produces a voltage which is approximately +20 volts at the plates of both CR805 and CR806, causing the junction of the two diodes to drop to approximately 20 volts where normally one of the two one-shots had maintained this point at approximately +200 volts. The voltage divider consisting of R834, R835, and R863, which is returned to -250 volts, now produces a negative voltage at the grid (pin 7) of V810

turning the tube off and producing a positive pulse at pin 6, the output. After differentiation, this pulse drives a cathode follower, V808A, which is identical to the data cathode follower just discussed. A neon indicator at the plate, pin 6, of V810B indicates when SOW has been detected. The SOW gate will recognize the same set of circumstances for EOW, as this produces the same condition of the SOW one-shot time delay, ending before the incoming code burst allows the data one-shot to return to its quiescent state.

2-5. EOW is recognized in a similar manner as SOW. The EOW one-shot V807, is triggered on and off by the data one-shot which applies positive and negative pulses at its grid, pin 2. As this one-shot is set for a period exceeding that of the SOW one-shot, when a SOW burst occurs, it will not have completed its time delay before the data one-shot recovers from the SOW burst. On an EOW burst, the same circumstances are produced with the EOW one-shot as just described for the SOW one-shot. The data one-shot produces a negative pulse to the plate of diode CR807, as it did to CR806. The EOW one-shot produces a positive pulse to the plate of diode CR808. During data bursts, the EOW one-shot is triggered off by the data one-shot, and both pulses are of approximately the same width. When an EOW burst occurs, the data one-shot is kept on, and the EOW one-shot completes its time delay. This produces a negative pulse to the grid (pin 2) of V809A similar to that previously discussed for SOW. The output at pin 1 of V809 is a positive pulse for EOW recognition, which drives pin 7 of V809B, the EOW output cathode follower. This cathode follower is identical to the data and SOW cathode followers. A neon indicator is connected to the plate of V809A which indicates the detection of EOW.

2-6. Oscillator - The oscillator within the Data Line Amplifier provides a 1 kc sine wave synchronized to data, and is used by external sources as a means of determining the data bit rate, often referred to as clock. This is necessary as an accurate means of determining whether an absence of data represents one or more 0 bits.

2-6.1. The basic oscillator, V810A, is similar to a standard Colpitts configuration. The frequency is varied by adjusting variable inductor L803. The oscillator is synchronized to incoming data by V811B. Each time a data bit is recognized, one-shot V806 is triggered. Its output, a positive pulse at pin 6, pulses V811B through capacitor C816. Since inductor L803 is in series with the cathode of V811B, each time the tube is pulsed, current flowing through the tube also flows through L803, which is within the tuned circuit of the oscillator. The output of the oscillator, at pin 3, drives a cathode follower, V811A, whose output at pin 3 is a-c coupled to the output terminal, pin 7 of P801, as 1 kc output.

2-7. Power Supply - 115 vac enters the Data Line Amplifier at pins 34 through 37 of P801. DS801 indicates when power is on. The a-c power is connected through fuse F1 to the primary of transformer T802. A secondary, pins 3 and 5, provides 6.3 vac for tube filaments.

A secondary, pins 8 and 10, provides 600 vac center tapped at pin 9 to 0 volts. Three diodes in series are used for rectification to safely meet the voltage requirements. Diodes CR816 through CR821 provide full wave rectification for +250 volts. Resistors R873, R878, and R879 and capacitors C834A and C834B provide filtering. Regulation of the +250 volts is performed by two VR tubes in series, V814 and V815. Half wave rectification, via diodes CR822 through CR824, is used for -250 volts. Filtering and regulation are similar to the +250 volt supply.

2-8. Adjustment - Three basic types of adjustments are to be made on the Data Line Amplifier.

2-8.1. Oscillator - The oscillator frequency is adjusted to 1 kc by adjusting variable inductor L803. Before the oscillator can be properly adjusted, the synchronizing effect of incoming data must be removed. One method of accomplishing this is to adjust R801 until the center tap is at 0 volts. The oscillator no longer receives sync pulses and is then in a free-running condition. Using a dual-trace oscilloscope such as a Tektronix 545A with CA plug-in, synchronize and put one trace on a good 1 kc source. If a local source is not available, data from a Data Line Amplifier, preferably with an input test pattern of all "1"s offers a suitable source. Use the remaining trace to observe pin 3 of tube V810. L803 should be adjusted to produce a frequency equal to the test frequency. By ultimately using a sweep on the scope which displays only one or two cycles, the operator can insure that the two signals are actually at the same frequency.

NOTE

At relatively slow sweeps, the two waveforms may have the appearance of being synchronized. If going to a faster sweep results in double traces, the two waveforms are not yet synchronized.

Rolling of one trace with respect to the other should be expected, but it is readily possible to adjust the oscillator to within a few cycles per second of the external source. A normal adjustment of ±3 cps is satisfactory.

NOTE

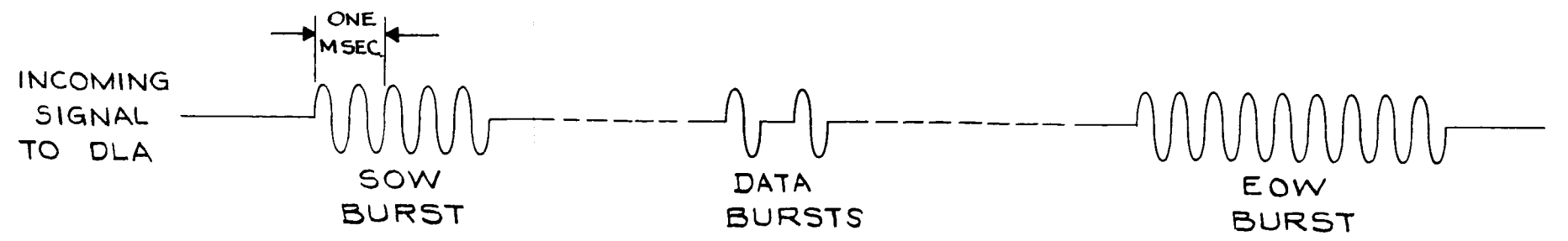
An alternate method of adjusting the oscillator using a frequency counter is acceptable.

2-8.2. Level and Detection - The ideal settings for the level and detection controls

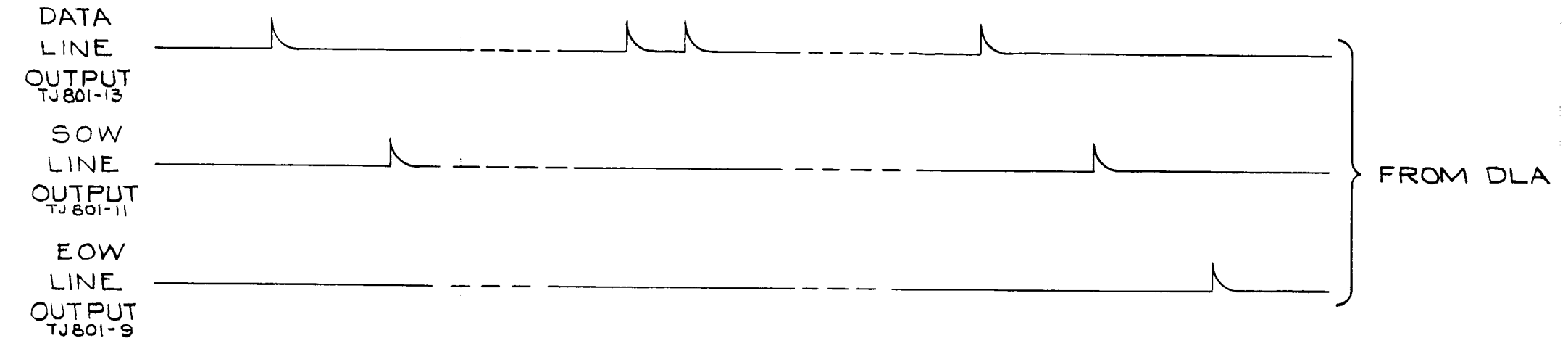
are best determined by examining the detected waveform output, TJ801-48. It is convenient for the remainder of the adjustments to use the delayed sweep feature of the oscilloscope. Using EOW, TJ801-9, as sync, and the delayed sweep, it is possible to examine incoming data occurring over a relatively long period at magnifications where the full sweep displays only a few milliseconds of data, and the scope still maintains sync on a stable source. The level and detection controls, potentiometers R801 and R822, should be adjusted until the detected waveform TJ801-48, has the appearance shown in the Data Line Amplifier Waveform Figure. The detected waveform is nominally a 15 to 20 volt negative pulse. It can be noted that for each bit of data, the ideal waveform produces two negative pulses, each with full amplitude, and squared at the bottom. It is also acceptable and common, due to frequency rolling, to have one of the two pulses of a lesser amplitude. It is unacceptable to have three pulses, specifically because the data one-shot is re-triggered on the third pulse making the output of V805 excessively wide. Proper adjustment, therefore, constitutes the obtaining of maximum amplitude and squareness of the detected signal without detecting three pulses for a data bit. If the adjustments have been made properly, one data pulse will appear at TJ801-13 for each data burst on the input at TJ801-50.

2-8.3. SOW and EOW One-Shots - The SOW and EOW one-shots are variable because the length of the SOW and EOW code bursts depend upon the system in which the Data Line Amplifier is used. These one-shots are normally set for a period that produces a pulse which is 0.5 milliseconds shorter than the incoming code burst for that signal. For example, if SOW is a 2.5 millisecond burst, the SOW one-shot is adjusted for 2 milliseconds. If EOW is a 4.5 millisecond burst, the EOW one-shot is adjusted for 4 milliseconds.

2-8.3.1. To properly adjust the SOW one-shot, using the delayed sweep of the oscilloscope as previously described, synchronize on EOW at TJ801-9 in the Data Line Amplifier. On one trace observe the data input, TJ801-50. On the remaining trace observe the SOW one-shot, TJ801-44. Adjust the time delay of the scope sweep until a SOW burst is seen. It is necessary to observe the one-shot pulse occurring during the SOW burst because during a data burst the SOW one-shot is triggered off by the data one-shot and not allowed to complete its time delay. Adjust potentiometer R849 to set the SOW one-shot for the desired width. Adjust the time delay of the scope until an EOW burst is seen. Observe the EOW one-shot, TJ801-46 and set potentiometer R843 for the desired width.

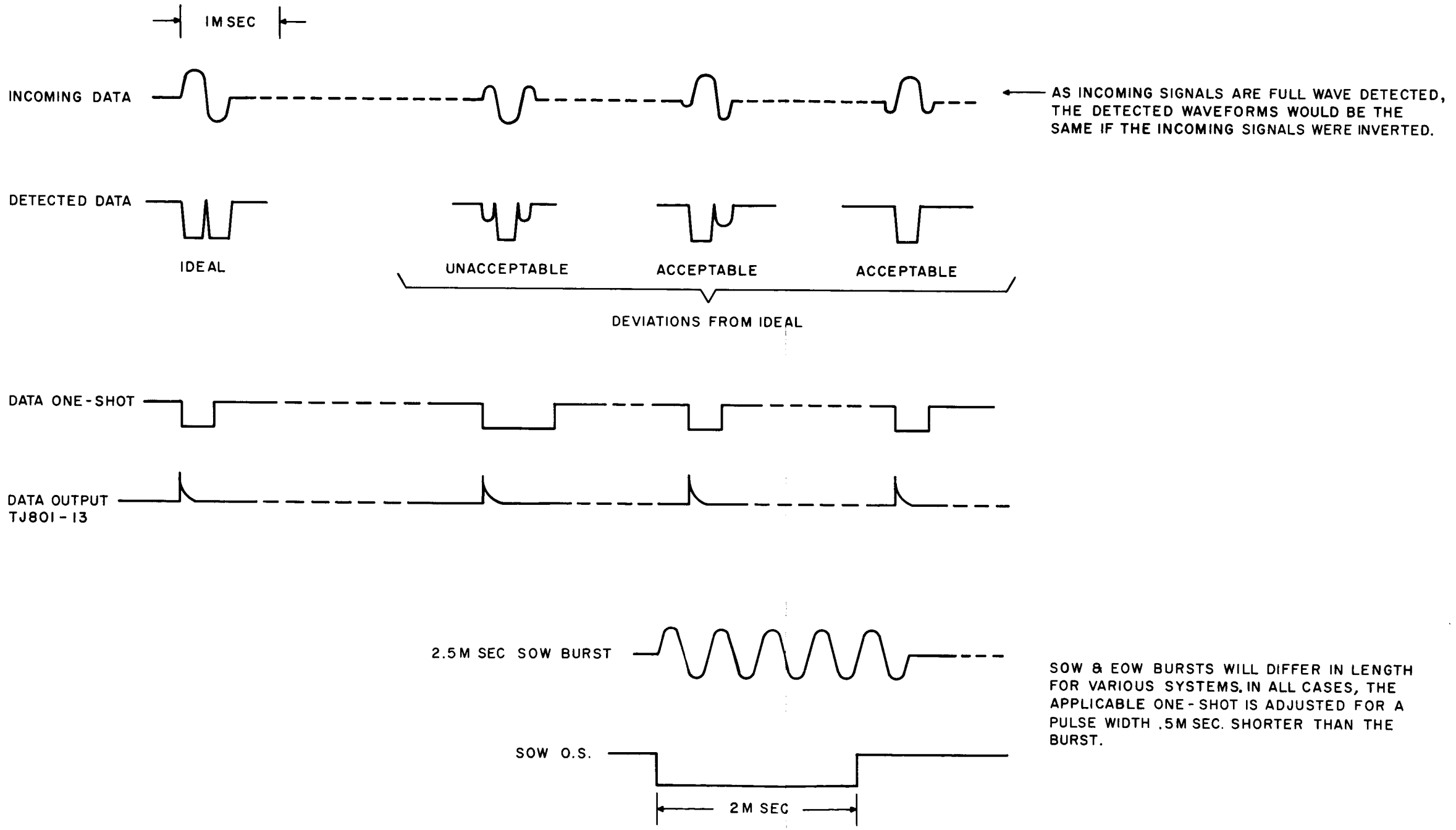


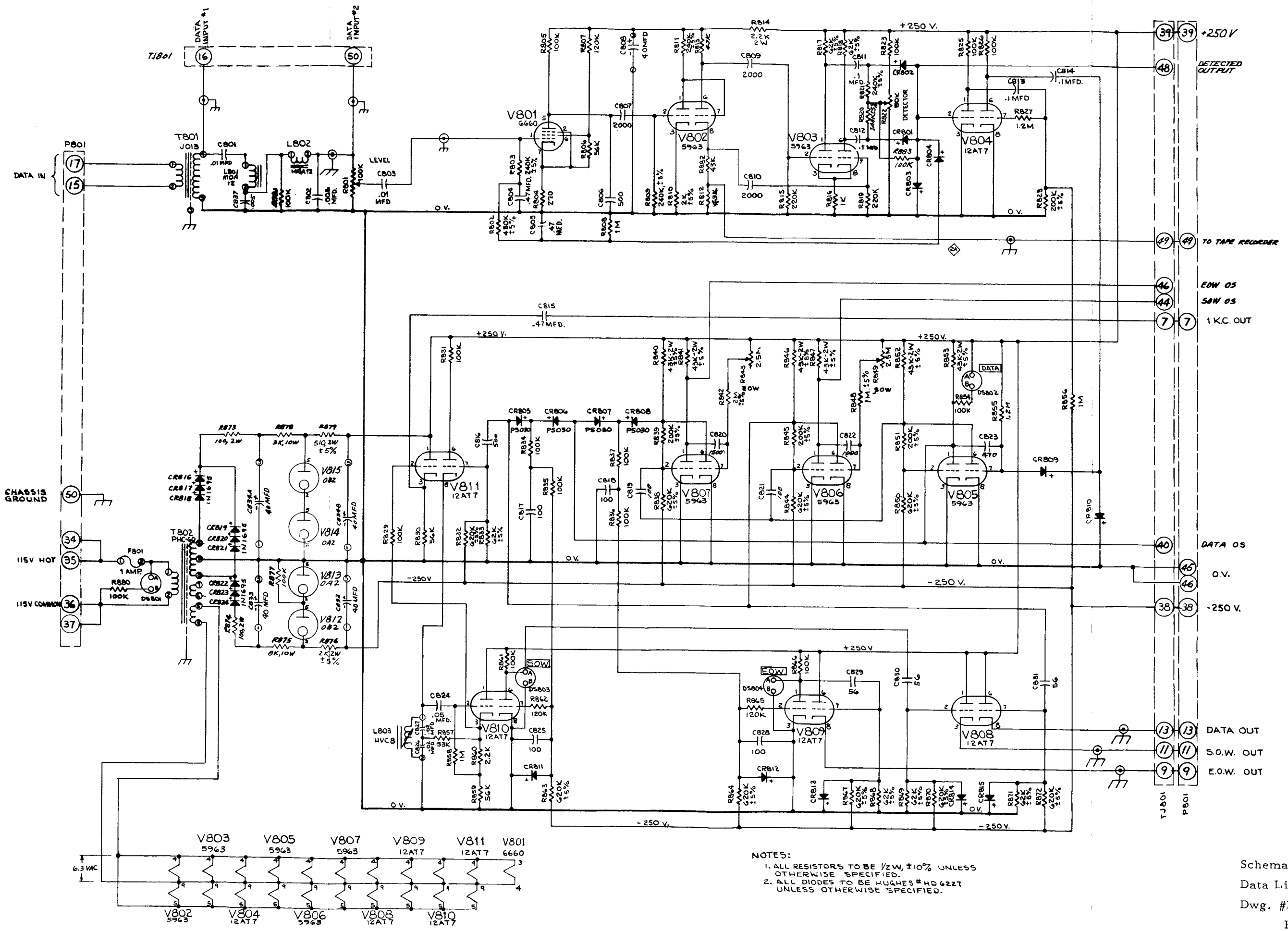
THIS FIGURE SHOWS THAT DATA PULSES ARE OBTAINED AT SOW & EOW - AND SOW PULSES ARE OBTAINED AT EOW.



NOTE:

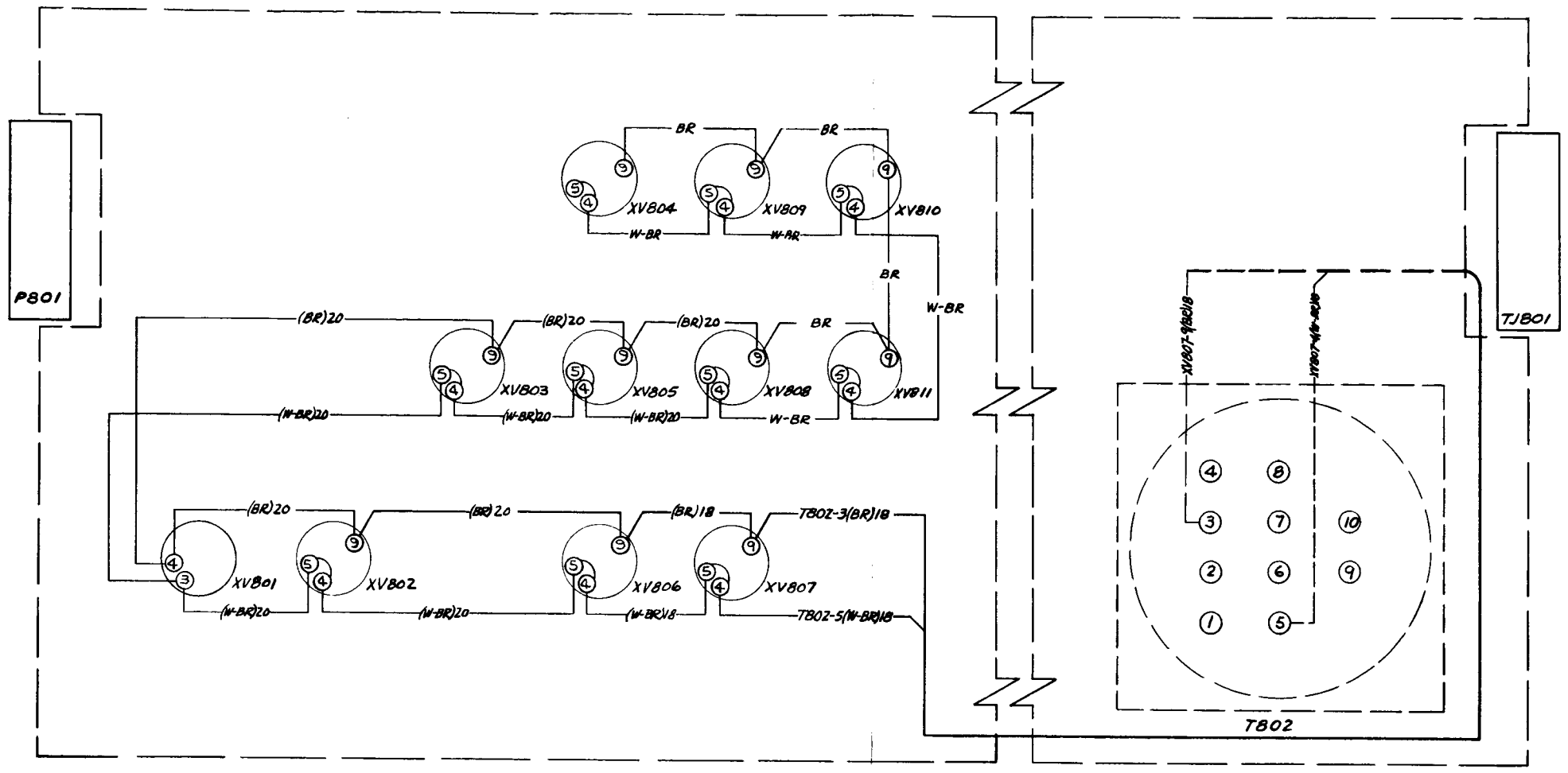
AMPLITUDES NOT DRAWN TO SCALE.
OUTPUT PULSES APPROX. 10 μSEC. WIDE AT HALF AMPLITUDE.
SOW & EOW BURSTS MAY VARY IN LENGTH DEPENDING UPON THE SYSTEM IN WHICH THEY ARE USED.
SOW & EOW OUTPUTS WILL NORMALLY OCCUR .5 M SEC. BEFORE THE END OF BURST.
IN SOME SYSTEMS, SOW AND/OR EOW ARE NOT NECESSARILY USED.


1M SEC
INCOMING DATA
AS INCOMING SIGNALS ARE FULL WAVE DETECTED, THE DETECTED WAVEFORMS WOULD BE THE SAME IF THE INCOMING SIGNALS WERE INVERTED.
DETECTED DATA
IDEAL
UNACCEPTABLE
ACCEPTABLE
ACCEPTABLE
DEVIATIONS FROM IDEAL
DATA ONE-SHOT
DATA OUTPUT TJ801-13
2.5M SEC SOW BURST
SOW O.S.
2M SEC
SOW & EOW BURSTS WILL DIFFER IN LENGTH FOR VARIOUS SYSTEMS. IN ALL CASES, THE APPLICABLE ONE-SHOT IS ADJUSTED FOR A PULSE WIDTH .5M SEC. SHORTER THAN THE BURST.



NOTES:
1. ALL RESISTORS TO BE 1/2W, ±10% UNLESS OTHERWISE SPECIFIED.
2. ALL DIODES TO BE HUGHES # HD 6227 UNLESS OTHERWISE SPECIFIED.

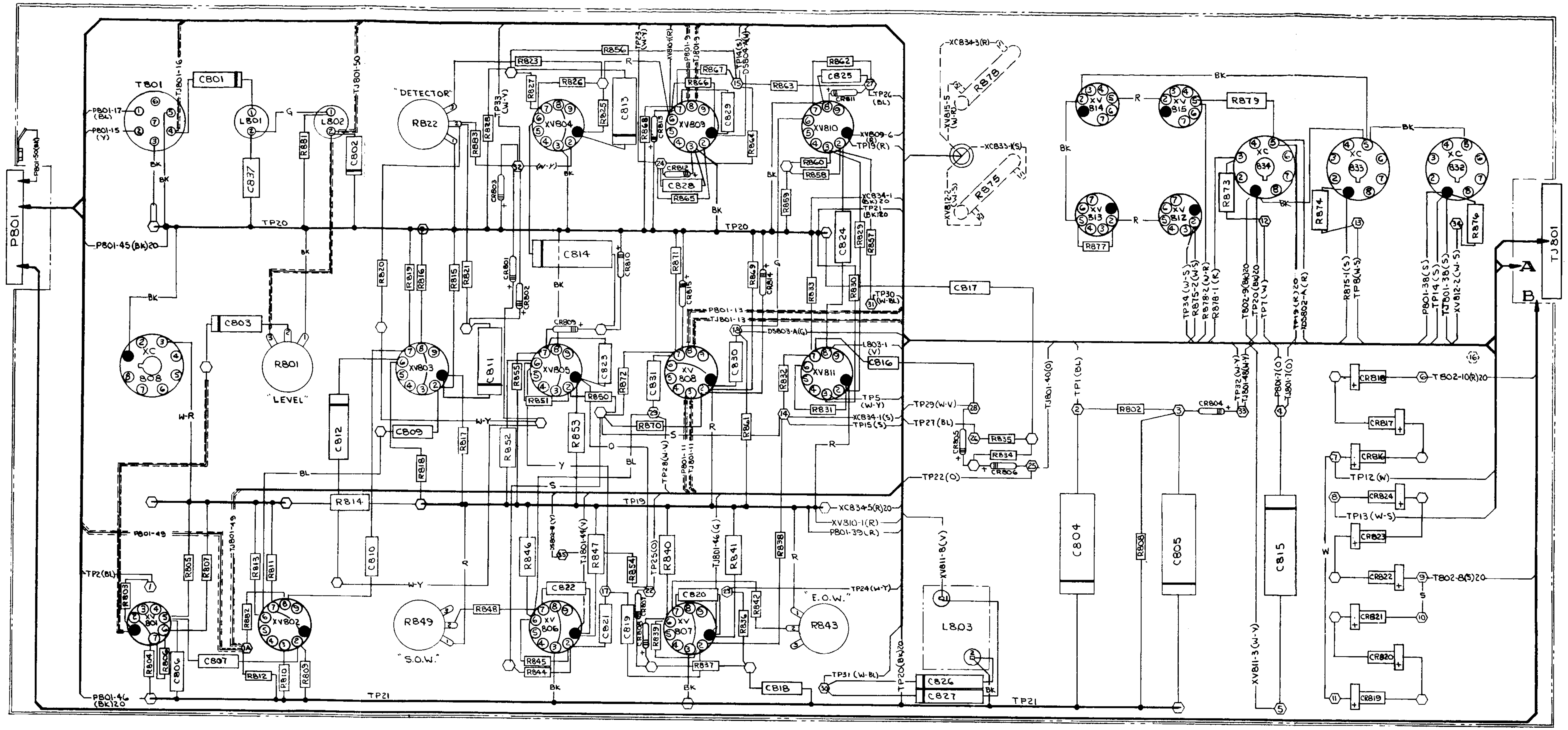
Schematic,
Data Line Amplifier
Dwg. #D71S8A



NOTES:

1. ALL WIRES TO BE #22 GA. UNLESS SPECIFIED.
2. ALL FILAMENT WIRES TO BE TWISTED PAIRS.

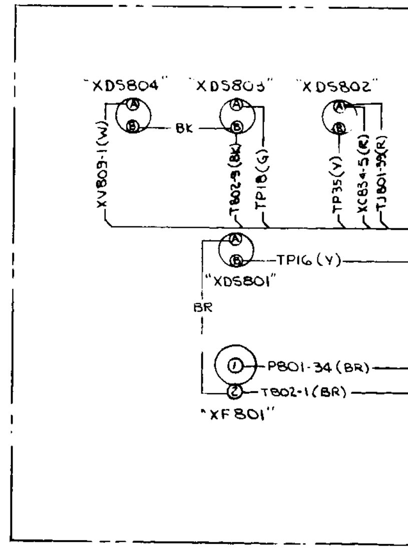
Wiring Diagram,
Data Line Amplifier
Dwg. #C71W8A



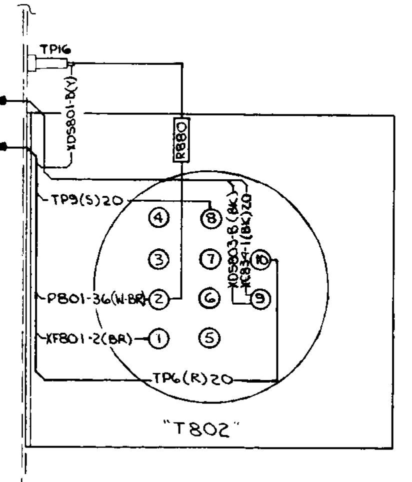
P801			
PIN	DESTINATION	FUNCTION	WIRE
7	TP4	1 K.C. OUT	O
9	XV809-8	E.O.W. OUT	COAX
11	XV808-3	S.O.W. OUT	COAX
13	XV808-8	DATA OUT	COAX
15	T801-2	DATA IN	Y.
17	T801-1	DATA IN	BL
34	XF801-1	115 VAC HOT	BR
35		115 VAC HOT	
36	T802-2	115 VAC COM	W-BR
37		115 VAC COM	
45	TP20	O V.	(BK) 20
46	TP21	O V.	(BK) 20
49	TP1A		COAX
50	GND LUG	CHASSIS GND	BK
38	XC832-1	-250 V	S
39	TP19	+250 V	R

JUMPER TERMINALS 34 & 35, 36 & 37, 45 & 46

TJ801			
PIN	DESTINATION	FUNCTION	WIRE
7	TP4	1 K.C. OUT	O
9	XV809-8	E.O.W. OUT	COAX
11	XV808-3	S.O.W. OUT	COAX
13	XV808-8	DATA OUT	COAX
16	T801-4	DATA INPUT #1	COAX
38	XC832-1	-250 V	S
39	XDS802-A	+250 V	R
40	TP25	DATA-O.S.	O
44	XV806-1	S.O.W.-O.S.	V
46	XV807-1	E.O.W.-O.S.	G
48	TP33	DETECTOR OUTPUT	W-Y
50	L802-2	DATA INPUT #2	COAX
49	TP1A		COAX



FRONT PANEL
(REAR VIEW)



TRANSFORMER
(FRONT VIEW)

NOTES:
1. ALL WIRE TO BE #22 GA UNLESS OTHERWISE SPECIFIED.
2. ~~~~ DESIGNATES COAX TYPE RG 174/U.
3. GROUND ONE END ONLY OF ALL COAX LEADS.
4. GROUND CENTER POST OF ALL 7 & 9 PIN SOCKETS.
5. FOR FILAMENT WIRING SEE DWG. #C71W8A, SH. #2

Wiring Diagram,
Data Line Amplifier
Dwg. #D71W8A

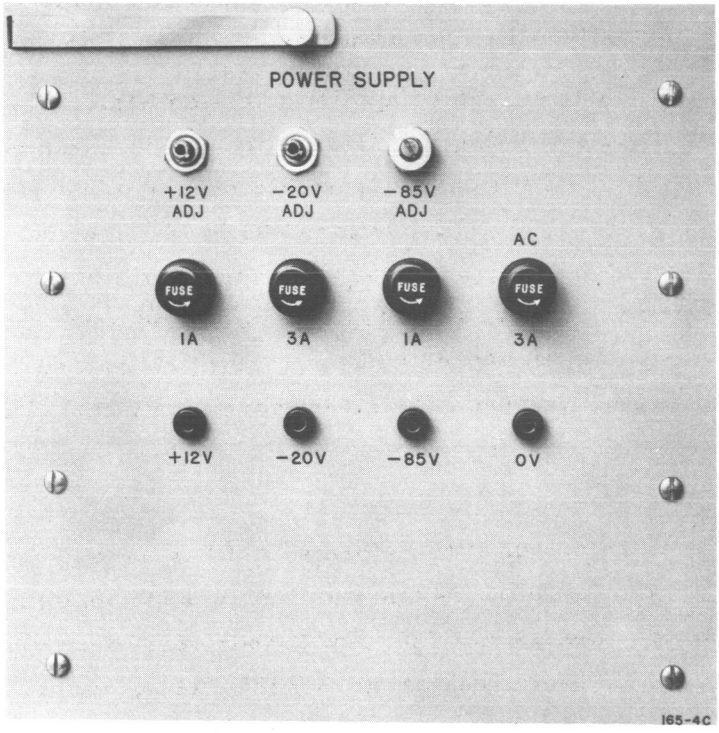
TRANSISTOR POWER SUPPLY
MEC MODEL 165-4 C

1. GENERAL DESCRIPTION

A Milgo type 165-4C Power Supply has three outputs: the first, a +12v, (+1v, -3v) at 1 ampere output; the second, a -20v, (+2v, -6v) at 2 amperes output; and the third, a -65v (±5v) at one ampere output. The -65v supply is stacked on the bottom of the -20v supply, thereby giving an output of -85v. The a-c input of this supply can vary from 100vac to 130vac and from 45 to 60 cycles. The unit is mounted in a standard Milgo slide-type rack and has a front panel 8-3/4 inches high by 8-7/8 inches wide. Its weight is approximately 35 pounds.

2. +12v SUPPLY

2-1. A portion of the output of transformer T401 is rectified by a bridge rectifier CR401 and filtered by resistor R401 and capacitors C401 and C402. The voltage across capacitors C401 and C402 is normally 20v (approximate). Transistor Q401 and resistors R402 and R403 act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q401 is decreased so that the IR drop across R402, R403, and Q401 will remain constant producing a constant output voltage. If the input a-c line voltage should increase, the d-c voltage across filtered capacitors C401 and C402 would increase and the effective resistance of Q401 must increase again so that the output voltage will remain constant.



Transistor Power Supply

2-2. The effective resistance of Q401 is controlled by the control section, consisting of transistors Q402, Q403, Q404, and their associated circuitry. Q404 determines whether the output voltage is too high or too low and is followed by power amplifiers Q403 and Q402, which amplify the control signal to the necessary power level for driving Q401. The base voltage of Q404 is referenced from the output of 4.7v zener diode CR402. The emitter voltage of Q404 is determined by the resistor divider network of R413, R414, and R415. The voltage from the wiper of potentiometer R414 is applied to the emitter of Q404.

2-3. As the output voltage increases, the magnitude of the voltage from the wiper of R414 will also increase proportionally. Since the output across zener diode CR402 remains constant as the output voltage increases, the emitter voltage tends to go positive with respect to the base voltage, driving Q404 toward cutoff. As Q404 goes toward cutoff, there is less collector current through R410, so there is less base current in Q403. The emitter current of Q403 decreases, reducing the current through R407 and base current of Q402. With less base current in Q402, the emitter current decreases, reducing the base current of Q401. With less base current, the effective resistance of Q401 will increase. Therefore, the output voltage decreases until Q404 senses the correct relationship between the output voltage and the zener voltage of CR402.

2-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q404 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q404, which increases the base current of Q403, thus increasing the emitter current of Q403 and the base current of Q402. This in turn increases the emitter current of Q402 and the base current of Q401, which reduces the effective resistance of Q401, causing the output voltage to return to its regulated value. Q404 actually is matching the zener voltage to the emitter voltage.

2-5. Since a portion of the output voltage applied to the emitter of Q404 can be varied by potentiometer R414, and the emitter voltage of Q404 is to remain constant, the output voltage must be changed as the resistor R414 is changed. In this manner, the regulated output voltage can be adjusted over a range of +9v to +13v. Capacitor C403 has been added to prevent hunting. Resistors R402 and R403 are included to limit the peak current through transistor Q401 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q401 and Q402. Resistor R404 provides a path for the leakage current of Q402 so that this current does not affect the base current in Q401, allowing Q401 to be more nearly cut off during a light load.

3. -20v SUPPLY

3-1. A second portion of the output of transformer T401 is rectified by bridge rectifier CR421 and filtered by parallel resistors R421A and R421B, and capacitors C421, C422, and C423. The d-c voltage across capacitors C421, C422, and C423 is 30v (approximate). Transistors Q421 and Q422 with their associated resistors R423, R424, and R422 act as a variable resistance element in series with the output load, which can be varied to maintain a constant

output voltage across a variable load. As the load current increases, the effective resistance of Q421 and Q422 is decreased so that the IR drop across R422, R423, R424, Q421, and Q422 will remain constant, producing a constant output voltage.

3-2. If the input a-c line voltage should increase, the d-c voltage across filter capacitors C421, C422, and C423 would increase, and the effective resistance of Q421 and Q422 must increase again to keep the output voltage constant. The effective resistance of Q421 and Q422 is controlled by the control section, consisting of transistors Q423, Q424, and Q425 and their associated circuitry. Transistor Q425 determines whether the output voltage is too high or too low and is followed by power amplifiers Q424 and Q423, which amplify the control signal to the necessary power level for driving Q421 and Q422. The base voltage of Q425 is referenced from the output by a 4.7v zener diode CR422. The emitter voltage of Q425 is determined by a resistor divider network R434, R435, and R436. The voltage from the wiper of potentiometer R435 is applied to the emitter of Q425.

3-3. As the output voltage increases, the magnitude of the voltage from the wiper of R435 will increase proportionally. Since the output across CR422 remains constant as the output voltage increases, the emitter voltage tends to become positive with respect to the base voltage, driving Q425, which is an NPN transistor, toward cutoff. As Q425 goes toward cutoff, there is less collector current through R431, and consequently, there is less base current in Q424. With less base current in Q424, the emitter current of Q424 decreases. With less emitter current in Q424, the current through R428 and the base current of Q423 also decrease. This reduces the emitter current in Q423 and reduces the base current in Q421 and Q422. Less base current in Q421 and Q422 increases their effective resistance, which increases the IR drop across them. Therefore, the output voltage decreases until Q425 senses the correct relationship between the output voltage and the zener voltage of CR422.

3-4. Conversely, if the output voltage decreases below the desired value, the portion of the output voltage applied to the emitter of Q425 also decreases, tending to make the emitter more negative with respect to the base. This increases the collector current of Q425, increasing the base current of Q424, which in turn increases the emitter current of Q424 and the base current of Q423. This, in turn, increases the emitter current of Q423 and the base current of Q421 and Q422, reducing the effective resistance of Q421 and Q422, and causing the output voltage to return to its regulated value. Transistor Q425 is actually matching the zener voltage to the emitter voltage.

3-5. Since a portion of the output voltage applied to the emitter of Q425 can be varied by potentiometer R435, and the emitter voltage of Q425 is to remain constant, the output voltage will have to be changed as the resistor R435 is changed. In this manner, the regulated voltage of this supply can be adjusted from -14v to -22v. Capacitors C425 and C424 provide feedback for stabilization purposes.

3-6. Resistors R423 and R424 serve two functions. First, they force the collector current of Q421 and Q422 to balance. Since the bases are tied in common, if one transistor conducts

more than the other, the higher IR drop in their associated resistor would tend to reverse bias the transistor with the most current and, in this manner, force the currents to balance. Second, if the output supply is shorted, resistors R422, R423 and R424 limit the peak current through Q421 and Q422 to a safe value while fuse F402 is melting. Resistor R425 provides a path for the leakage current of Q423 so that this leakage current does not affect the base current in Q421 and Q422. This allows Q421 and Q422 to be more nearly cut off during a light load.

4. -65v SUPPLY

4-1. A third portion of the output of transformer T401 is rectified by a bridge rectifier CR441 and filtered by resistor R441 and capacitors C441 and C442. The voltage across capacitor C441 and C442 is normally 75v (approximate). Transistor Q441, and resistors R442 and R443, act as a variable resistance element in series with the output load, which can be varied to maintain a constant output voltage across a variable load. As the load current increases, the effective resistance of Q441 is decreased so that the IR drop across R442, R443, and Q441 will remain constant, producing a constant output voltage. If the input a-c line voltage increases, the d-c voltage across filtered capacitors C441 and C442 will increase and the effective resistance of Q441 must increase again so that the output voltage will remain constant.

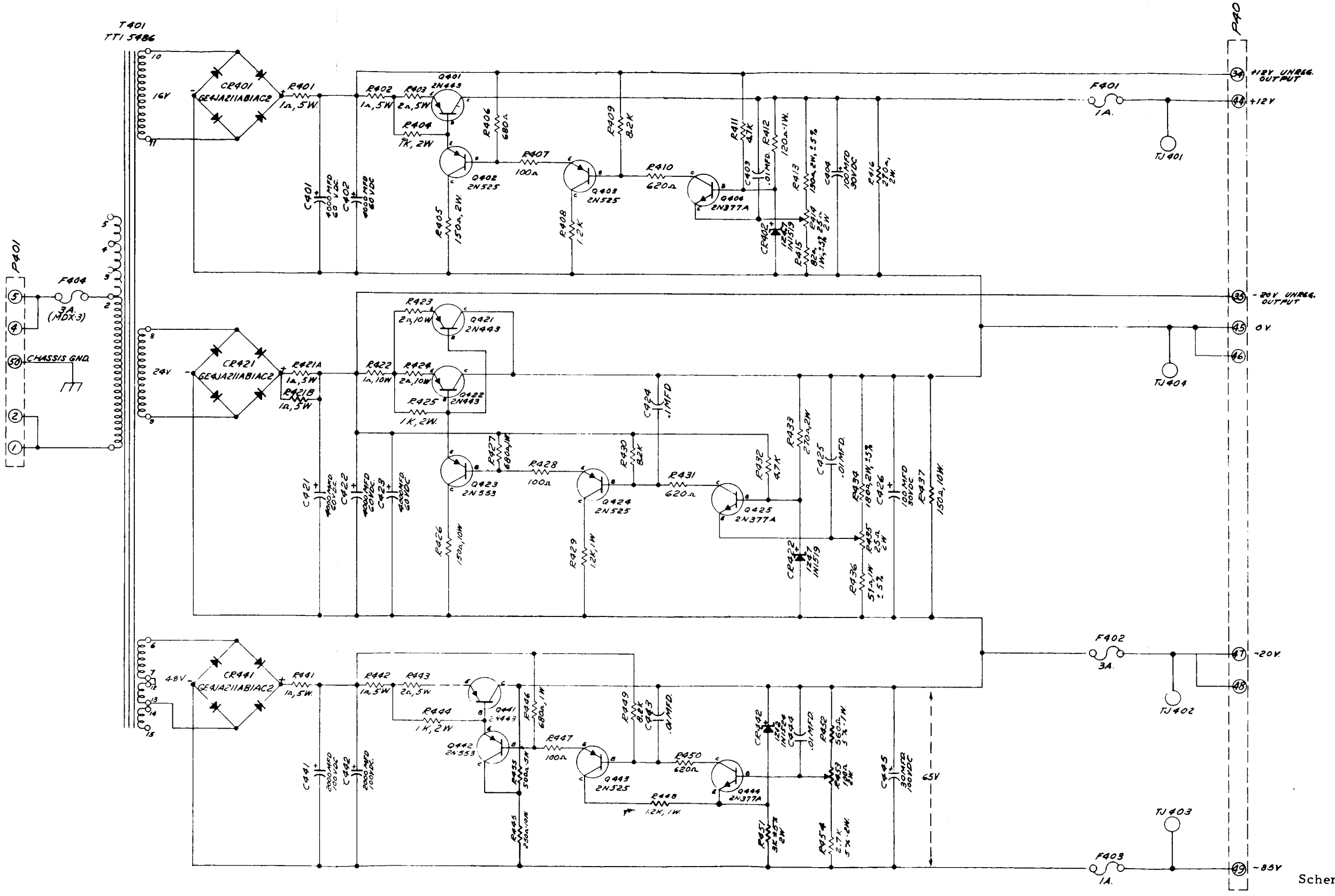
4-2. The effective resistance of Q441 is determined by the control section, consisting of transistors Q442, Q443, and Q444 and their associated circuitry. Q444 determines whether the output voltage is too high or too low and is followed by power amplifiers Q443 and Q442. These amplify the control signal to the necessary power level for driving Q441. The emitter voltage of Q444 is referenced from the output by a 12v zener diode CR442. The base voltage of Q444 is determined by the resistor divider network of R452, R453, and R454. The voltage from the wiper of potentiometer R453 is applied to the base of Q444. The zener is referenced from the positive side of this supply to reduce the emitter-to-collector voltage of Q443 and Q444 to less than 25v.

4-3. As the output voltage increases, the magnitude of the voltage from the wiper of R453 will also increase proportionally. Since the output across zener diode CR442 remains constant as the output volts increase, the base voltage tends to become negative with respect to the emitter voltage, driving Q444 toward cutoff. As Q444 goes toward cutoff, there is less collector current through R450 and less base current in Q443. The emitter current of Q443 decreases, reducing the current through R447 and the base current of Q442. With less base current, the Q442 emitter current decreases, reducing the base current of Q441. With less base current, the effective resistance of Q441 increases. Therefore, the output voltage decreases until Q444 senses the correct relationship between the output voltage and the zener voltage of CR442.

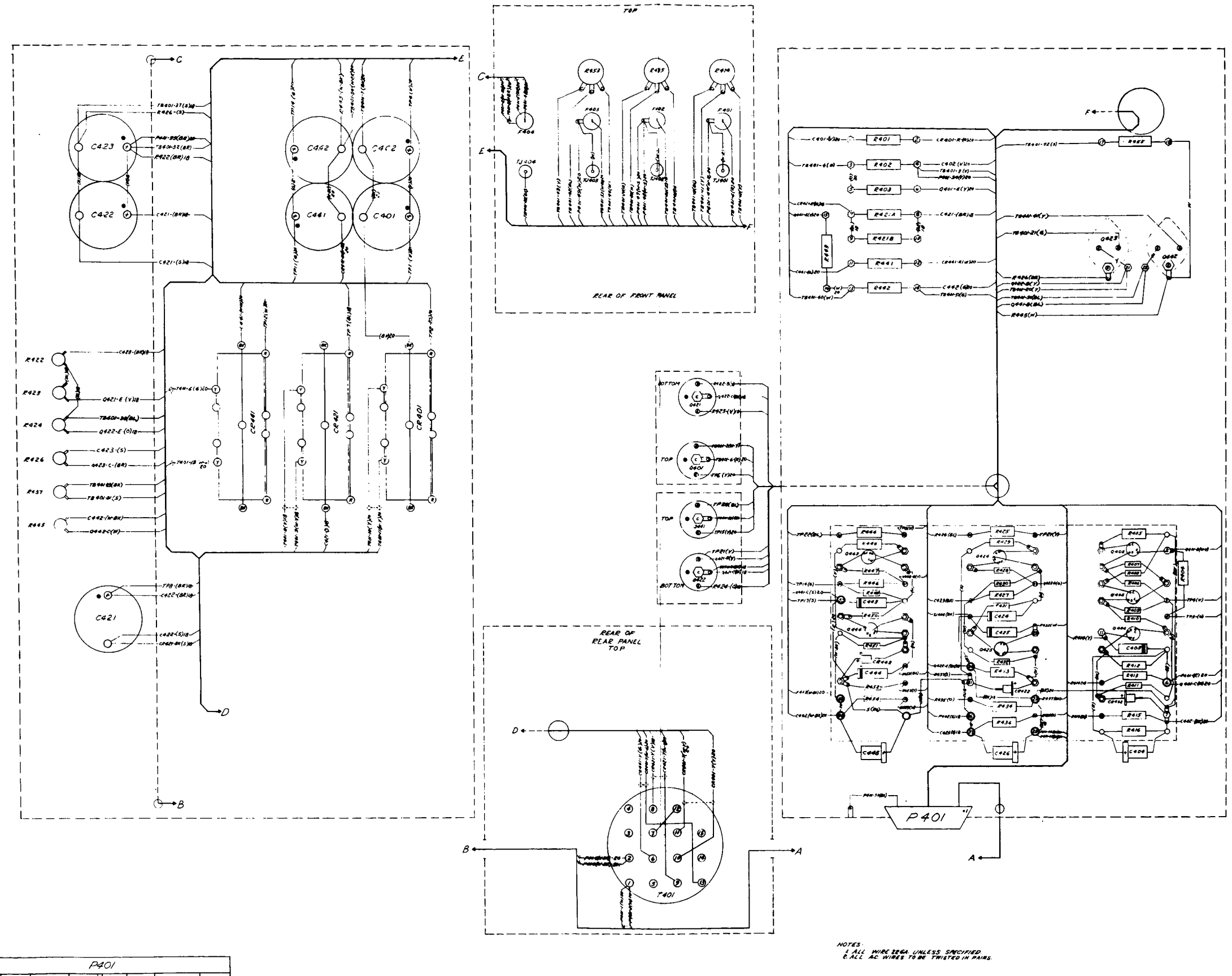
4-4. If the output voltage decreases below the desired value, the portion of the output voltage applied to the base of Q441 also decreases, tending to make the base more positive

with respect to the emitter. This increases the collector current of Q444, increasing the base current of Q443, and increasing the emitter current of Q443 and the base current of Q442. This in turn increases the emitter current of Q442 and the base current of Q441, reducing the effective resistance of Q441, and causes the output voltage to increase and to return to its regulated value. Q444 is actually matching the zener voltage to the base voltage.

4-5. Since a portion of the output voltage applied to the base of Q444 can be varied by potentiometer R453, and the base voltage of Q444 is to remain constant, the output voltage will have to be changed as the resistor R453 is changed. In this manner, the regulated output voltage can be adjusted over a range of -60v to -70v. Capacitors C443 and C444 have been added to prevent hunting. Resistors R442 and R443 are included to limit the peak current to transistor Q441 to a safe value if the output terminal is short circuited, and to provide reverse bias for Q441. Resistor R444 provides a path for the leakage current of Q442 so that this current does not affect the base current in Q441. This allows Q441 to be more nearly cut off during a light load. This -65v power supply is stacked on the bottom of the -20v supply giving a combined output of -85v.



Schematic
165-4C Power Supply
Dwg. #D165S4C



P401								
PIN	DEST.	FUNCTION	WIRE	PIN	DEST.	FUNCTION	WIRE
1	P401-1	AC INPUT	(W) 20	41			
2	T401-1	AC INPUT	(W) 20	42			
3				43			
4	P406	AC INPUT	(BK) 20	44	P401	+12 V	(W-R)20
5	P404	AC INPUT	(BK) 20	45	[illegible]	0 V	(BK) 20
6				46	T401-2	0 V	(BK) 20
7				47	P402	-20 V	(W-B)20
8				48	P402	-20 V	(W-G)20
49	[illegible]		(W) 20	49	P402	-AAV	(W)20
50	[illegible]		(W) 20	50	CHASSIS	CHASSIS GND	(BK)

Wiring Diagram
165-4C Power Supply
Dwg. #E165W46

MAGNETIC CORES

1. GENERAL

A component commonly used in digital data handling equipment is a magnetic core. The term magnetic core is usually applied to a small torroid composed of magnetic material which has high permeability and also high retention. This material will have what is called a square hysteresis loop, shown in Point A, Figure MN-1. Because of this square hysteresis loop, there are two stable energy states, which make the cores adaptable to digital circuits. Magnetic cores are commonly used for shift registers, "and" gates, "or" gates, and other logic circuits, in addition to their use as blocking oscillator transformers.

2. THEORY OF OPERATION

2-1. GENERAL

a. The action of a magnetic core can best be described by referring to the drawing of the hysteresis loop (Figure MN-1). The magnetomotive force, or ampere-turns, applied to the winding of a core is measured along the X axis. Magnetic flux density (gausses), or flux lines per square centimeter, is being measured along the Y axis. Once a core has been magnetized and had this magnetization reversed several times, the relationship between flux density and magnetomotive force is described by the hysteresis loop in Figure MN-1.

b. With no current going through any of the core windings, the flux density will be either at point D or at point H, depending upon the direction in which the core has most recently been saturated. If the core is assumed to be at point D on the hysteresis loop and ampere-turns are applied in the negative direction, the relationship between the flux density and the magnetomotive force will follow the line DE. If additional ampere-turns are applied in the negative direction, the core will go on to condition F, at which point saturation has occurred and additional ampere-turns of magnetomotive force will result in only a minor increase in flux level to point G.

c. If the current through the windings is now removed, the core will return to point H on they hysteresis loop. Even though there are no ampere-turns, there is still a flux density proportional to OH in the core. The characteristics of the core material are such that this

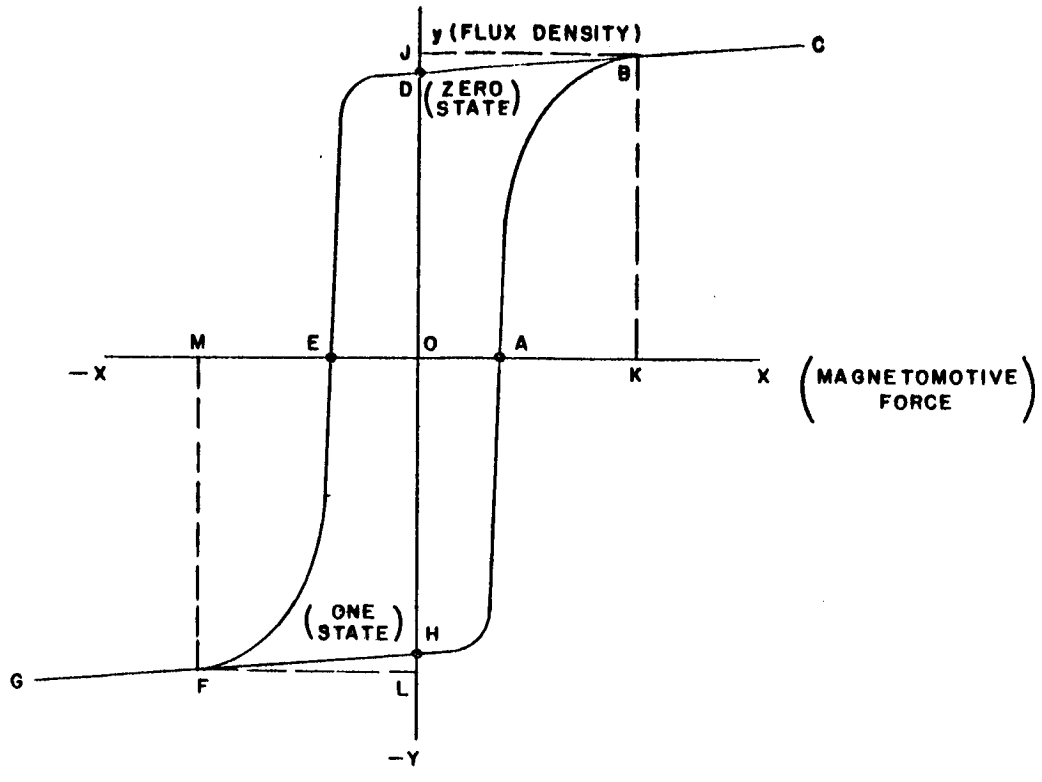


Figure MN-1. Square Hysteresis Loop

flux density will remain indefinitely as though it were a permanent magnetic. If the direction of current in the winding is reversed, positive ampere-turns are applied. This will move the condition of the core from H to A and on to B, at which point the core is now saturated in the positive direction and additional ampere-turns of magnetomotive force will cause very little change in flux density to point C. When the current in the coil is removed, the core will now go from C to D, where it will remain indefinitely until driven again.

d. The net change in flux, when going from a negative quiescent state to plus saturation, is proportional to HJ. It should be noted that other windings on the magnetic core will sense this change in flux and will generate a voltage proportional to the number of turns and the rate of change of flux. Figure MN-2 shows a simple magnetic core with three windings on it. If positive ampere-turns are then applied to winding No. 1, the core condition effectively goes from D to B. Since the hysteresis loop is very square, the change in flux during this time (proportional to DJ) is very small when compared to HJ. As a result, the voltage generated in coil No. 2 will be very small at this time.

e. If negative ampere-turns are again applied so that the core goes from D to E to F, the

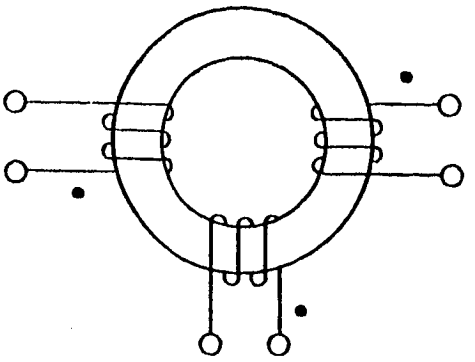


Figure MN-2. Simple Magnetic Core

change in flux will be proportional to DL. The voltage generated in winding No. 2 will now be equal in magnitude, but opposite in polarity, to the voltage generated in that winding when the core went from H to B. These pulses can be separated with diodes and used for different purposes in logic circuits. The two stable states, D and H, are referred to as the "0" state and the "1" state respectively.

2-2. MN11 MAGNETIC CORE

a. A Milgo MN11 magnetic core has four windings and associated components designed specifically for shift register application (Figure MN-3). Pin 7 is connected to a -25v supply. The core drive pulse, applied to pin 1, travels from -25v to approximately zero volts and return, with a rise time no greater than 5 microseconds and a fall time no greater than 10 microseconds. The pulse width must be at least 10 microseconds at 50 percent of measured points, but is normally approximately 40 microseconds wide.

b. This positive going pulse applied to pin 1 results in ampere-turns driving the core beyond positive saturation (Point C in Figure MN-1). When the core drive pulse has passed, the core is left in state D, which is defined as "O" state. The voltage at pin 8 is normally maintained at -25v but is raised to approximately -16v to insert a "1" into the core. It can be seen that the current in the input winding, as a result of a positive going pulse applied to pin 8, will magnetize the core in an opposite direction to that of the drive pulse. The state of the core will go from D to G on the hysteresis loop (Figure MN-1), and when the input pulse is passed, the core remains at H, which is defined as a "1" state.

c. When the next drive pulse occurs, the flux will travel from point H to Point C, and

transformer action of the core and windings will result in a positive pulse being generated at the dot end of all four windings. This positive pulse will be approximately 9v in magnitude with a rise time of approximately 6 microseconds. Once the core has gone from negative saturation to positive saturation, there will be no more flux change even though the drive pulse is still present, and no additional voltage is generated in the windings. This switching time, which takes place in approximately 6 microseconds, determines the width of the pulse generated by the windings.

d. The 9v pulse generated in the advance winding causes diode CR3 to conduct, and will charge capacitor C3 to approximately -16v. After the core has switched to positive saturation, the voltage at pin 6 will revert to -25v. Diode CR3, however, prevents capacitor C3 from discharging through the advance winding, so the charge is held on C3 until it discharges through an external load.

e. During a core drive pulse, the voltage at pin 2 jumps from -25v to approximately zero volts because of the IR drop in R1 caused by the shift current. With pin 2 at approximately zero volts, diode CR2 will be reverse biased and no current can flow from pin 8 through CR2 and the input winding. After the core drive pulse has passed, the -16v charge on one CR3 can now discharge through CR2 and the input windings of the next core, driving it to the "1" state. A "1" can be inserted by raising pin 8 to -21v, or more positive. It should be pointed out that a "1" can also be inserted through pin 3, or by applying a pulse to pin 5, which becomes approximately 8v positive with respect to pin 4. If there is no "1" inserted between core drive pulses, the next core drive pulse will drive the core from point D to point C on the hysteresis loop, resulting in a very small change in flux density. This will result in a very small voltage being generated in the windings (approximately 0.5v), giving a signal-to-noise ratio of approximately 18 to 1.

f. It should be noted that energy transferred to a load while shifting out a "1" comes from the core driver and not from the core. The energy in the core merely allows energy to be transferred to the output winding while the core is acting as a transformer. The Milgo MN11 operates equally well on a power supply voltage of -20v instead of -25v as described.

2-3. SHIFT REGISTERS

a. When connected to form a shift register, MN11 cores are connected as shown in Figure MN-3. If a positive going pulse is applied to pin 8 of the first core, a "1" will be inserted into that core. During the next core drive pulse, all of the cores will be pulsed simultaneously, since they are connected in parallel. The resultant 9v pulse from the advance winding

of the first core will charge the capacitor in the first core to approximately -16v. When the first core has switched from minus saturation to plus saturation, there will no longer be any voltage generated in the advance winding. CR3 of the first core will prevent the capacitor from discharging through the advance winding, however, and CR2 in the second core prevents this capacitor from discharging through the input winding of the second core. CR2 is reverse biased because of the IR drop in the resistor of the second core caused by the shift current.

g. When the shift pulse has passed, the pin 2 voltage of the second core will go back to -25v and the capacitor in the first core may now discharge through the input winding of the second core. The resultant current through the input winding is sufficient to drive the second core from point D to point G on the saturation curve, so that when C3 is completely discharged, the second core will be in a "1" state. While this second core was being switched from plus saturation to minus saturation, flux linkages were changing in all of the windings of this core, with the result that a voltage was generated in all of these coils with the dot end of the winding negative. Diode CR1 will prevent any current flow in the drive winding as a result of the generated voltage, and the diode CR3 will prevent any current flow in the advance winding as a result of this generated voltage.

h. During the next core drive pulse, core 2 is switched from minus saturation to plus saturation, resulting in the output capacitor of the second core being charged. After the second core drive pulse, the discharge current from this capacitor will insert a "1" into the third core and so on to the last one. Since both ends of the auxiliary winding are brought out, the auxiliary winding may be used to generate either a positive going or negative going 9v pulse. This auxiliary pulse will be approximately 9v in magnitude, with a rise time of six microseconds and a fall time of approximately one half microsecond. In addition, the auxiliary winding can be used to insert "1's" into the core by applying a suitable positive pulse to pin 5 or a suitable negative pulse to pin 4. Pins 2, 3, and 6 are brought out for additional flexibility in adapting the MN11 core to logic circuits.

2-4. BLOCKING OSCILLATORS

a. The use of transformers for blocking oscillators is common and widely understood. It is also possible to use a square loop magnetic core as a blocking oscillator transformer with some desirable results in control of pulse width. Figure MN-4 shows the connections of either an MN12 or an MN13 as used in a blocking oscillator.

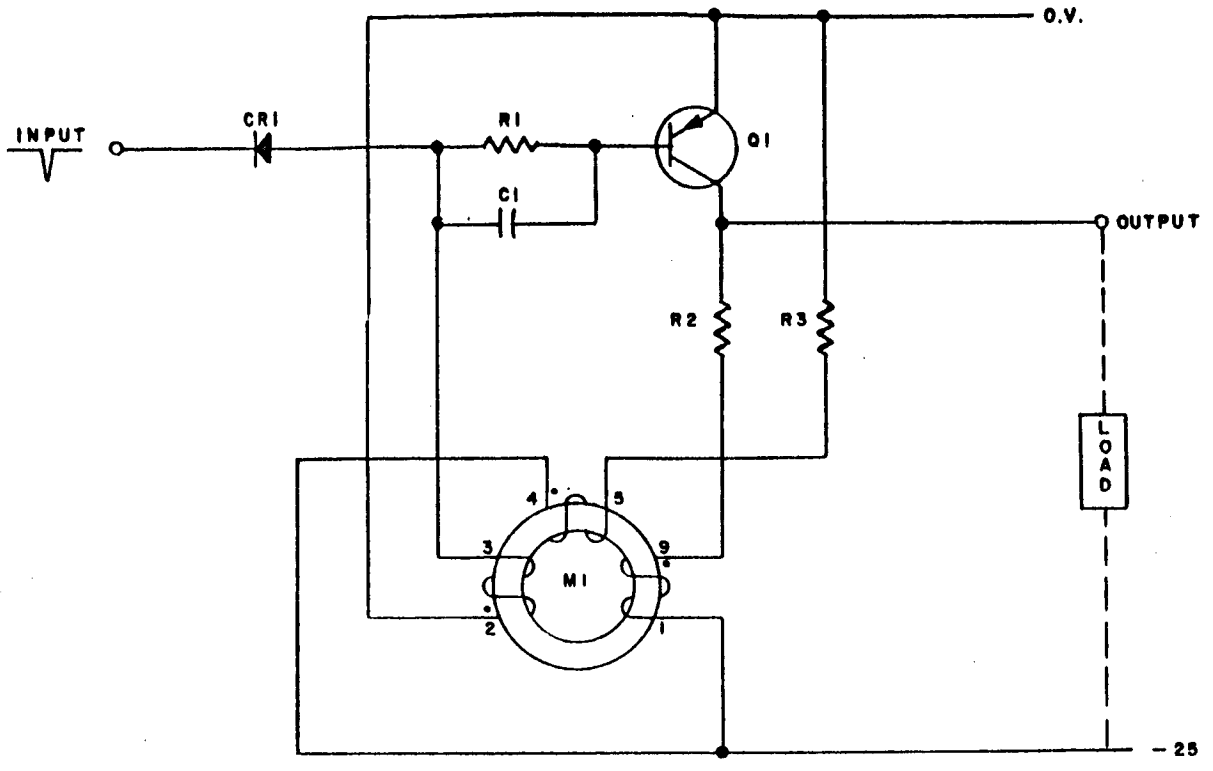


Figure MN-4. Blocking Oscillator (MN12 or MN13)

b. The 9-1 winding is the collector winding and could be compared to the primary winding of a transformer. The 2-3 winding is the feedback winding and could be compared to the secondary winding of a transformer. The 4-5 winding is the reset winding and has no counterpart in a conventional transformer. The reset winding is so connected that the current through the reset winding will drive the core into negative saturation. The transistor will normally be cut off, but when triggered by a negative pulse at the input, will go into conduction. The resulting collector current applies positive ampere-turns to the core and the flux moves from H toward A and B. The resulting flux change in the core is sensed by the feedback winding and a voltage is generated, making pin 3 negative. This negative going voltage is applied to the base of the transistor and drives the transistor into heavier conduction.

c. As the transistor conducts more heavily, the rate of change of flux increases, resulting in an even more negative voltage being applied to the base of the transistor. This feedback very quickly saturates the transistor (approximately one microsecond), but the collector current is limited by resistor R2 and the voltage generated in the collector winding of the core. As long as the core is still in the process of switching from minus saturation to plus

saturation, the core and its windings act as a transformer and the feedback winding continues to drive the transistor into saturation. When the core has finally reached saturation (B on hysteresis curve, Figure MN-1), additional ampere-turns from the collector winding will no longer result in a change of flux and no additional voltage will be generated in the feedback winding. This removes the drive to the transistor, which immediately cuts off, removing the ampere-turns from the collector winding.

d. Current through resistor R3 and the reset winding now starts to apply ampere-turns in the negative direction again and drives the core from position D to F. This results in a reversal of flux in the core, which reverses the voltage generated in the feedback winding. Pin 3 now becomes slightly positive, insuring a rapid cutoff of the transistor. Since the duration of the output pulse depends on the time it takes to switch the magnetic core, the pulse width depends on the core used and is relatively independent of the load on the blocking oscillator.

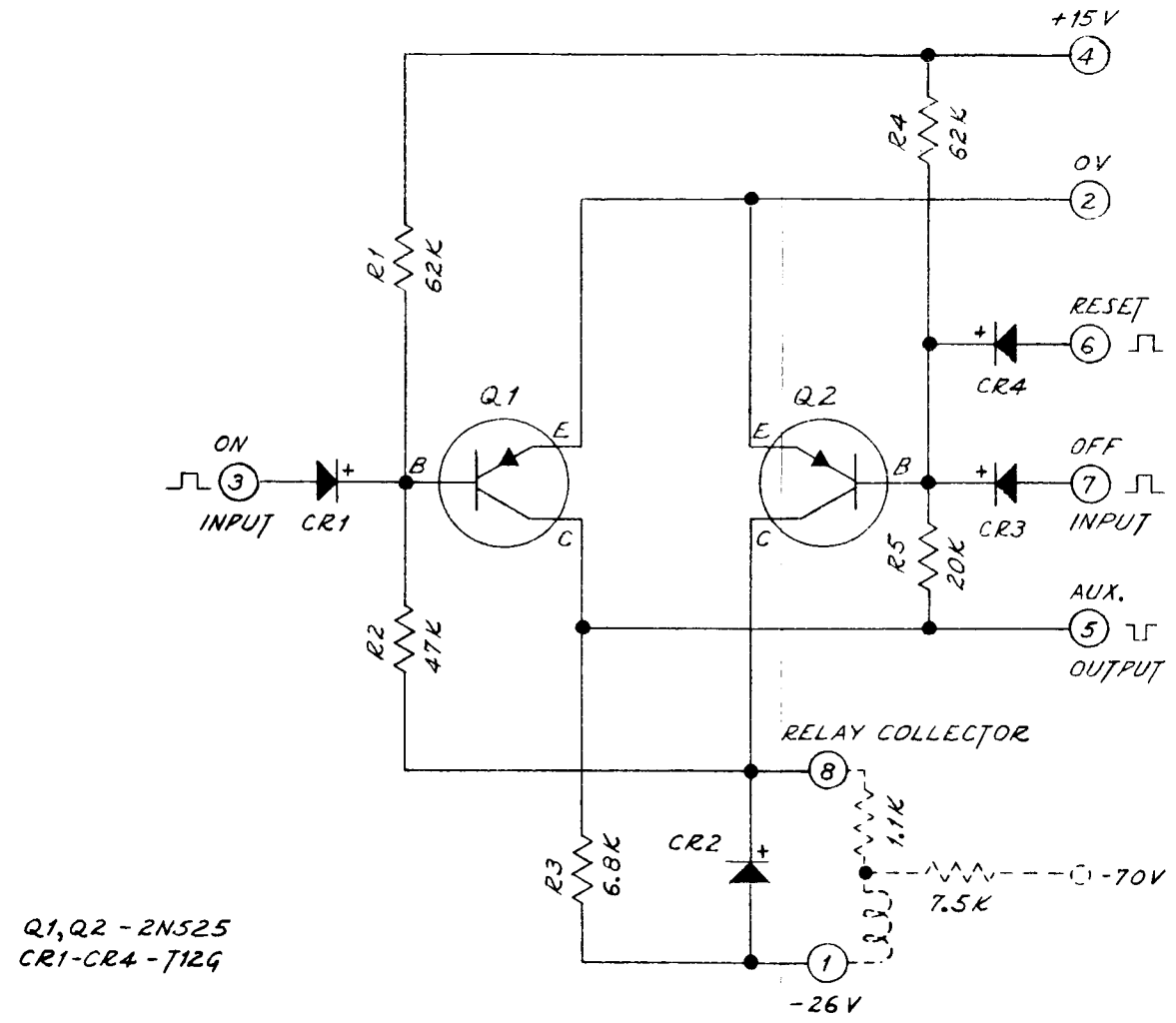
e. Two blocking oscillator cores are used in Milgo equipment: an MN12 and an MN13. The MN12 will cause a pulse approximately 10 microseconds wide to be generated by the blocking oscillator, while the MN13 will cause a pulse approximately 40 microseconds wide to be generated. It takes approximately 30 microseconds to reset an MN12 core and approximately 80 microseconds to reset an MN13 core.

C3
ADVANCE
CR3
AUX.
CR1
DRIVE
R1
160Ω
CR2
INPUT
CORE DRIVE
- 25

TN 28
RELAY DRIVING FLIP-FLOP

A TN28 is a bistable flip-flop which can be used for driving a relay coil or other loads of 500 ohms or more. The external load (shown on the schematic diagram in phantom between pins 8 and 1) is a special network used in conjunction with a 350 ohm relay coil which has permanent magnet bias and requires plus and minus currents for optimum operation. The network is normally defined as being in the "off" or "0" condition when transistor Q1 is saturated and Q2 is cut off, leaving the relay de-energized. The "on" or "1" condition is the opposite, with Q1 cut off and Q2 saturated, causing the relay to energize. Assuming that Q1 is saturated, then its collector is approximately -0.25 volts. Resistors R4 and R5 are then connected from +15 volts to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter at Q2 is at 0 volts, this reverse bias keeps Q2 cut off. With Q1 saturated, its base is at approximately -.05 volts; so the current through resistor R1 is approximately 0.25 milliamps. The current through the series combination of R2 and the external load resistor, which may very from 500 ohms to 5K, varies from 0.53 to 0.48 milliamps. The difference between the currents in R1 and R2 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition, so this condition is a stable one. The input voltages at pins 3, 6 and 7 must be somewhat negative during quiescent conditions. The flip-flop may be turned "on" by raising the voltage at pin 3 to a positive value so that diode CR1 conducts, raising the base voltage of Q1 to a positive value. Note that the input pulse will be loaded somewhat, so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off, R4 and R5 are no longer connected between 0 and +15 volts, and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R3, causing Q2 to saturate. Now resistors R1 and R2 are connected from +15 to 0 volts and hold the base of Q1 at approximately +6 volts, keeping Q1 in a cut off condition after the input pulse passes. This, then, is the other stable condition which will be maintained until Q2 is cut off by a positive pulse at either pin 6 or pin 7. A positive pulse at either of these pins turns Q2 off, allowing base current from Q1 to be conducted through R2 and the external load, driving Q1 back into saturation and restoring the initial condition. Diode CR2 is included to suppress the voltage of an external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cutoff, the relay coil is de-energized. However, the inductance of the relay coil attempts to maintain the current through the relay coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen, Q2 could be damaged by excessive emitter-collector voltage. To prevent this from happening, diode CR2 is added. During most phases of the cycle, CR2 is reverse biased and so does not enter into the operation of the circuit. When the relay is de-energized and pin 8 is driven negative by the relay inductance, CR2 is forward biased and conducts, providing a path for current through the relay coil

and eliminating the voltage spike. Although the description of operation of this network has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +12 volts and -20 volts or +10 volts and -15 volts.



Q1, Q2 - 2N525
CR1-CR4 - T12G

Schematic,

TN28 Relay Driving Flip-Flop

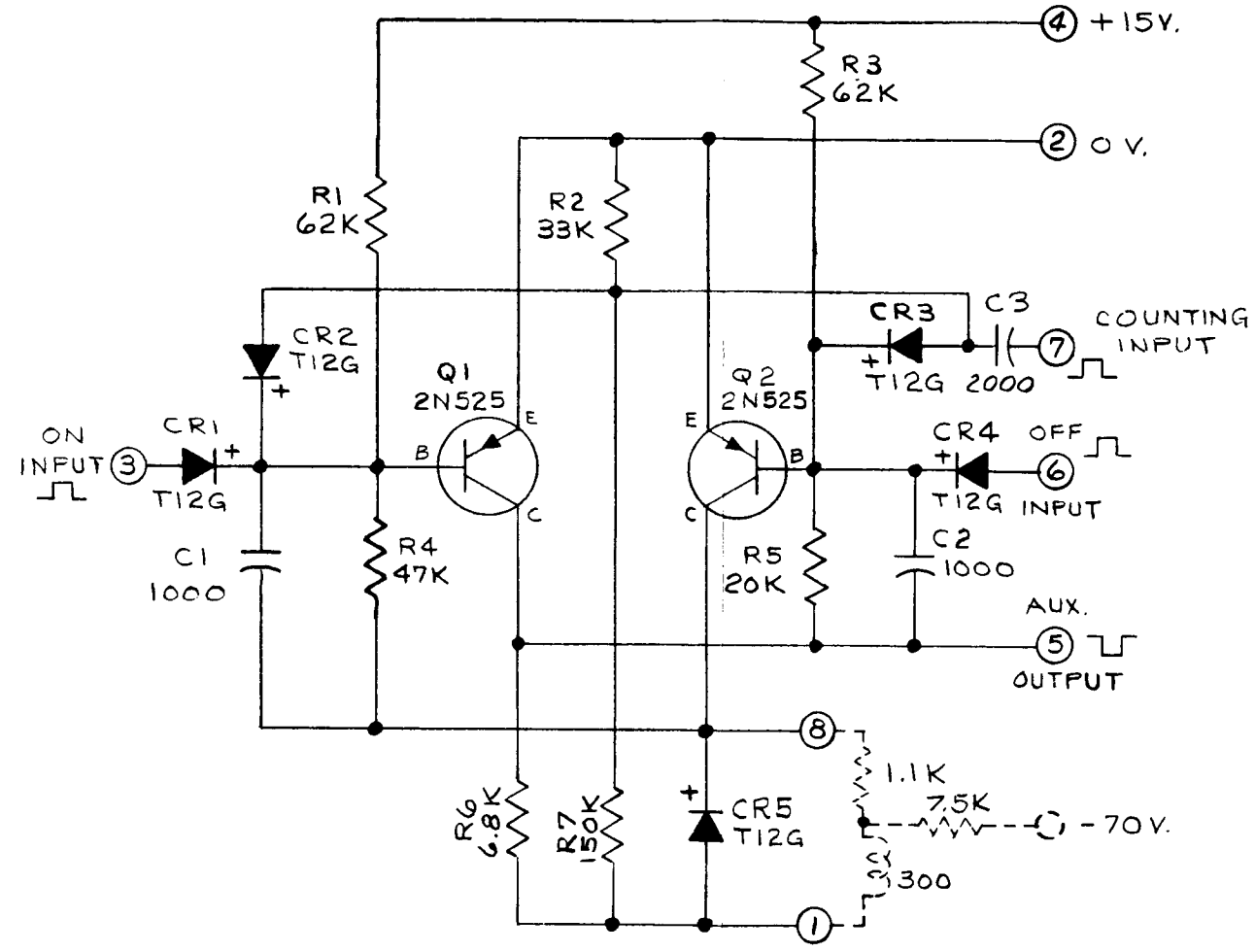
Dwg. #A103S28A

TN 42
RELAY DRIVING COUNTING FLIP-FLOP

TN42 is a counting type bistable flip-flop which can be used to drive a relay coil or other loads 500 ohms or more. The external load which is shown on the schematic diagram as dotted between pins 8 and 1 is a special network used in conjunction with a 350 ohm relay coil which has permanent magnet bias and requires plus and minus currents for optimum operation. The network is normally defined as being in the "off" condition when transistor Q1 is saturated and Q2 is cut off leaving the relay de-energized. The "on" or "1" condition is in the opposite, with Q1 cut off and Q2 saturated causing the relay to energize. If we assume that Q1 is saturated then its collector will be at approximately -0.25 volts. Resistors R3 and R5 are then connected from +15 to 0 volts and by divider action hold the base of Q2 at approximately +3.5 volts. Since the emitter at Q2 is at 0 volts, this reverse bias will keep Q2 cut off. With Q1 saturated its base will be at approximately -0.5 volts so the current through resistor R1 is 0.25 ma. The current through the series combination of R4 and the external load resistor, which may vary from 500 ohms to 5K, will vary from 0.53 to 0.48 ma. The difference between the current in R1 and the current in R4 is the base current of Q1, which is sufficient to drive Q1 to saturation. This satisfies the original condition, so that condition is a stable one. The input voltages at pins 3 and 6 must be somewhat negative during quiescent conditions. The flip-flop may be turned "on" by raising the voltage at pin 3 to a positive value so that diode CR1 will conduct, raising the base voltage of Q1 to a positive value. It should be noted that the input pulse will be loaded somewhat so it cannot be generated by a high impedance source. With the base of Q1 positive, Q1 is now reverse biased and cut off. With Q1 cut off R3 and R5 are no longer connected between 0 volts and +15 volts and Q2 is no longer clamped off. Instead, Q2 base current may now flow through resistors R5 and R6 causing Q2 to saturate. Now resistors R1 and R4 will be connected from +15 to 0 volts and will hold the base of Q1 at approximately +6 volts, keeping Q1 in a cut off condition after the input pulse passes. This then is the other stable condition, which will be maintained until Q2 is cut off by a positive pulse at pin 6. A positive pulse at pin 6 will turn Q2 off, allowing the base current from Q1 to be conducted through R4 and the external load, driving Q1 back into saturation and restoring the initial condition. Diode CR5 is included to suppress an external relay coil connected across pins 8 and 1. As Q2 goes from saturation to cut off the relay coil is de-energized. However, the inductance of the relay coil will attempt to maintain the current through the relay coil by driving the voltage at pin 8 much more negative than the -26 volt supply. If this were allowed to happen Q2 could be damaged by excessive emitter-collector voltage. To prevent this from happening, diode CR5 is added. During most phases of the cycle CR5 will be reverse biased and therefore will not enter into the operation of the circuit. But when the relay is de-energized and pin 8 is driven negative by the relay inductance, CR5 is now forward biased and conducts, providing a path for current through the relay coil

and eliminating the voltage spike.

The actions just described cover the operation of this network as a conventional bi-stable flip-flop which requires a turn-on pulse and a turn-off pulse. In addition, this network can be used for counting by using the pin 7 input. R2 and R7 act as a divider network which establishes their junction at -4.5 volts. Since the bases of Q1 and Q2 are either at -0.5 volts or at a positive voltage, both CR2 and CR3 will normally be reverse biased and non-conducting. By applying a positive pulse approximately 10 volts high with a rise time of approximately 0.5 microseconds to pin 7, the junction of R2 and R7 will be raised to +5.5 volts until C3 discharges. This will permit both CR2 and CR3 to conduct, which will cut off both Q1 and Q2 simultaneously. Assume the condition before the input pulse was Q1 saturated and Q2 cut off. When both are cut off by the input pulse there will be no drop in voltage at the collector of Q2, hence no pulse coupled through C1. But when Q1 cuts off the resulting drop in voltage at the Q1 collector is coupled through C2 to the base of Q2. The result is that when the input pulse has been differentiated (C3 charges up) and no longer has an effect, C2 forces Q2 to conduct. When the next positive pulse is applied to pin 7, the resulting drop in voltage at the Q2 collector will force Q1 to turn on first. In this way the state of the network will change from a "0" to a "1" or reverse for every positive pulse that is applied to pin 7.



Schematic,

TN42 Relay Driving Counting Flip-Flop

Dwg. #A103S42A

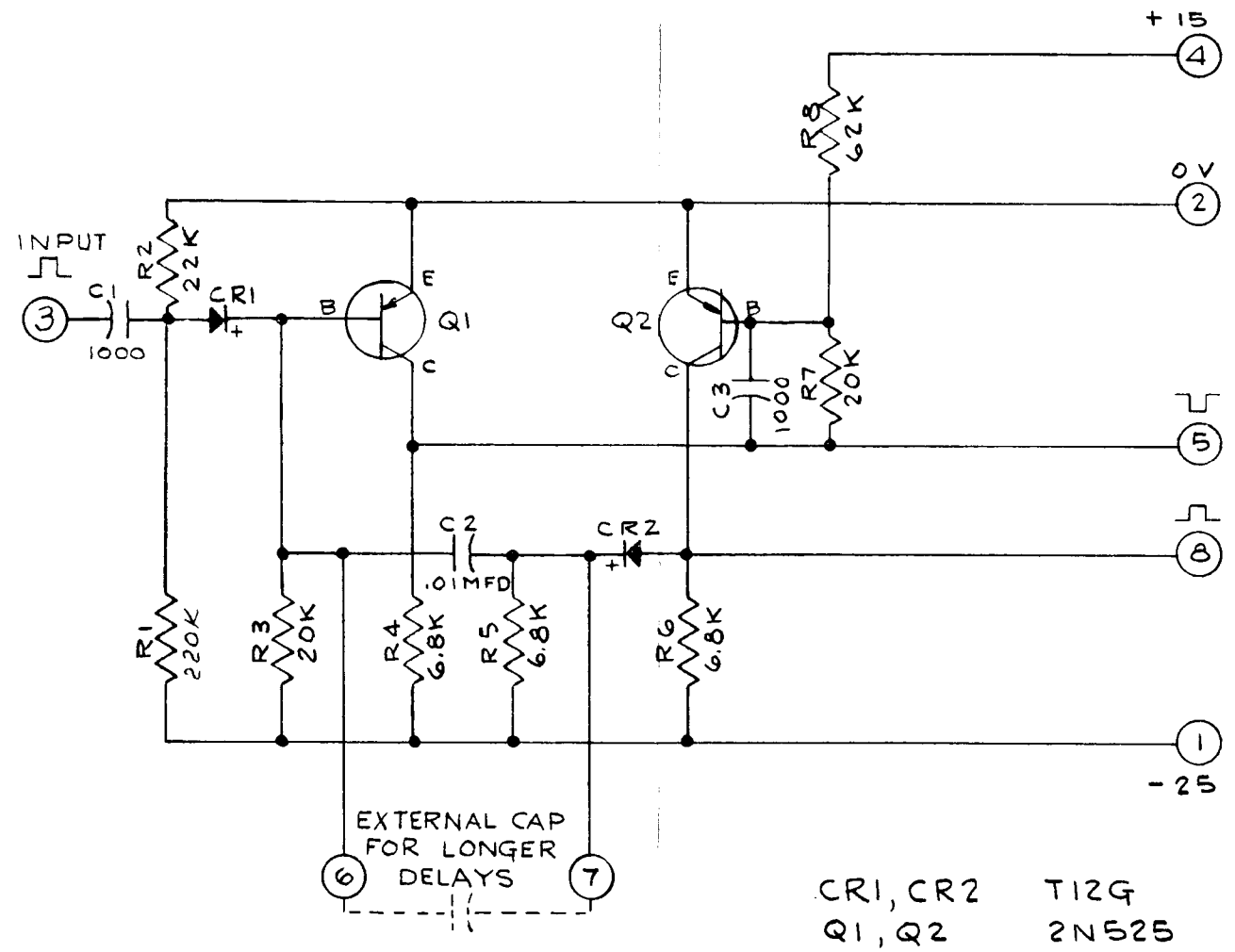
TN 51
ONE-SHOT (MONOSTABLE MULTIVIBRATOR)

The TN51 is a one-shot (monostable multivibrator) used for generating a pulse, variable in width from a minimum of 160 microseconds to over 2 milliseconds. In the quiescent condition, transistor Q1 is saturated by the base current through resistor R3. Since transistor Q1 is saturated, voltage divider R7 and R8 is connected between +15 volts and 0 volts, establishing a positive reverse bias voltage on the Q2 base and keeping Q2 cut off.

Resistors R1 and R2 form a voltage divider, establishing a noise bias of approximately -2.5 volts, so that normal input noise does not trigger the network. A positive pulse of not less than 10 volts, with a rise time not greater than 4 microseconds, will trigger the network by cutting off transistor Q1. Transistor Q1 is cut off when the input pulse raises the base voltage of transistor Q1 above 0 volts. Capacitor C1 is used to differentiate the input pulse so that a long duration input pulse will not affect the length of the output pulse.

With Q1 cut off, resistors R4 and R7 provide a path for the base current of transistor Q2, and Q2 saturates. The collector voltage of transistor Q2 will rise from -25 volts almost to 0 volts. This rise of voltage is coupled to the base of transistor Q2 via capacitor C2, keeping transistor Q1 at cut off until the R-C time of capacitor C2 and resistor R3 allows the base voltage of transistor Q1 to return below 0 volts. Q1 saturates again and cuts off Q2.

This time can be lengthened by adding capacitance in parallel with capacitor C2. The terminals of C2 are brought out on pins 6 and 7 of the network. CR2 is used to decrease the fall time of the output pulse by preventing C2 from discharging through R6. Resistor R5 provides a d-c path for the current of C2. This network will operate on lower supply voltages such as +12 volts and -20 volts, or +10 volts and -15 volts.



CR1, CR2 T12G
Q1, Q2 2N525

Schematic,

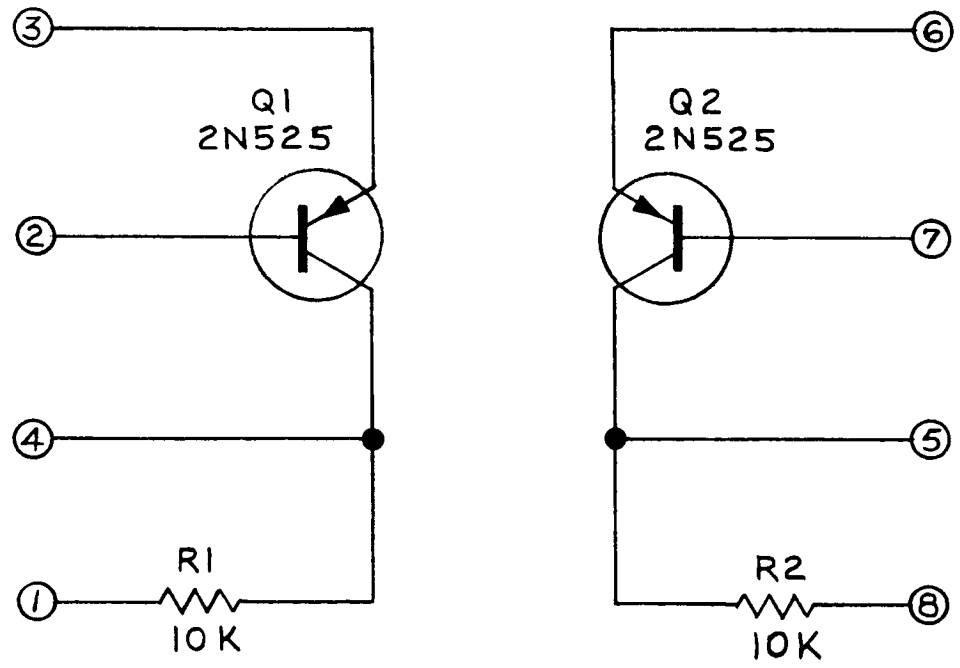
TN51 One-Shot (Monostable Multivibrator)

Dwg. #A103S51A

TN 57
DUAL PULSE AMPLIFIER

The TN57 contains two PNP transistors connected as two independent conventional amplifiers. Only one of these will be discussed since the other is identical to it. As normally used, a supply voltage is connected to pins 3 and 1 with the plus side on pin 3. Pin 2 will be the input and pin 4 the output. As long as pin 2 is more positive than pin 3 the transistor is cut off and the voltage at pin 4 will be the same as the voltage at pin 1. When pin 2 is approximately 0.5 volts negative with respect to pin 3 the transistor will saturate and the voltage at pin 4 will go positive until it saturates, approximately 0.25 volts more negative than the emitter. Caution must be used to connect an external base resistor in series with pin 3 to prevent damage to the transistor. The value of the external base resistor is dependent upon how negative the driving voltage goes and upon the external load that is connected to pin 4. To insure saturation the base current should be at least 1/20th of the collector current.

The TN57 may also be used in a variety of applications by the addition of external components.

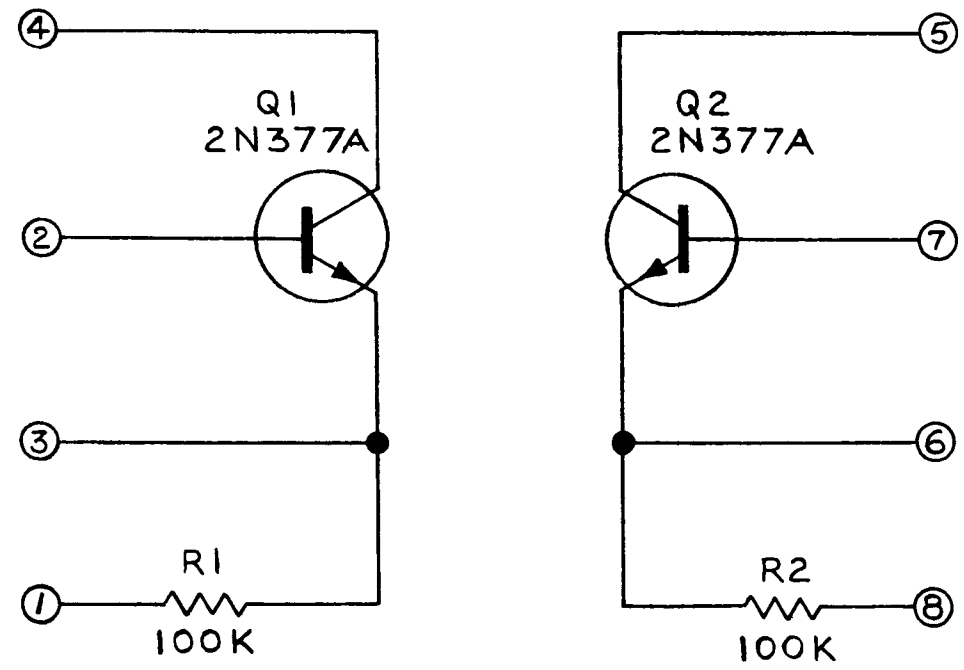


Schematic
TN57 Dual Pulse Amplifier
Dwg. #A103S57A

TN 58
DUAL EMITTER FOLLOWER

A TN58 consists of two NPN transistors connected as independent emitter followers. As normally used, a supply voltage is connected to pins 4 and 1 with the plus side on pin 4. As the voltage at pin 2 is varied, between the voltages at pins 4 and 1, the transistor will conduct and the voltage at the emitter, pin 3, will be approximately 0.4 volts more negative than the voltage at pin 2. Because of the power gain of the transistor a lower impedance load can be driven from pin 3 than could have been driven from the signal applied to pin 2.

The TN58 may also be used in a variety of applications by the addition of external components.



Schematic
TN58 Dual Emitter Follower
Dwg. #A103S58A

TN 130 B
CORE DRIVER

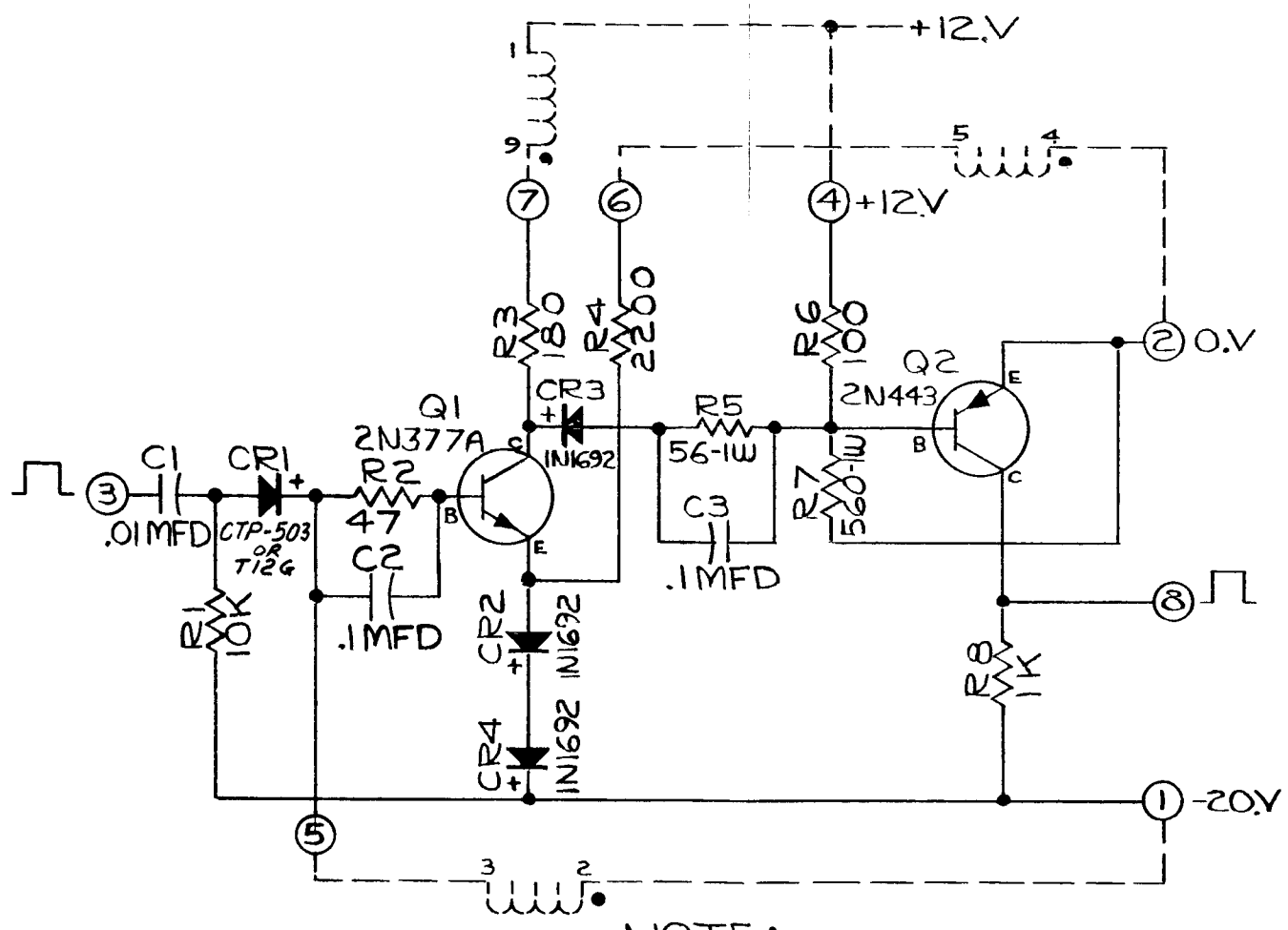
The TN130B is a blocking oscillator with amplifier which generates a positive going pulse from -20 volts to 0 volts, with a time duration determined by the core with which it is used. The TN130B is normally used with a MEC Model MN13 core, which gives it a pulse width of approximately 40 microseconds.

In the quiescent condition, transistor Q1 is maintained in cut off. The emitter voltage of Q1 is determined by the forward voltage drop of diodes CR2 and CR4 (1.5 volts) and is at approximately -18.5 volts. The base of Q1 is returned to -20 volts through R2 and the feedback winding of the core, connected from pin 5 to -20 volts. The d-c impedance of the feedback winding is approximately 5 ohms; thus the base of Q1 is nearly -20 volts, keeping Q1 reverse biased approximately 0.7 volts and properly cut off. Since there is no Q1 collector current, the collector voltage is +12 volts.

A positive going input pulse at pin 3 is coupled by capacitor C1, diode CR1, and capacitor C2, paralleled with R2 to the base of Q1. This pulse starts Q1 conducting. The resulting Q1 collector current passes through the collector winding of the external core. This generates a voltage across the collector winding coupled through the core to the feedback winding. By noting the phasing of the windings on the core, it can be seen that, as the collector voltage becomes negative, the voltage at pin 5 is becoming positive. This in turn drives Q1 further into conduction, even after the input pulse has been differentiated by C1. Q1 saturates in approximately one microsecond with an emitter-collector voltage of approximately 0.25 volts. Q1 will remain saturated as long as transformer action in the core continues to drive pin 5 of the TN network sufficiently positive to cause Q1 base current to flow. The pulse width (approximately 40 microseconds for an MN13 core) is determined by the characteristics of the core.

When the core material finally reaches saturation, transformer action in the core will cease, the feedback winding will no longer drive pin 5 positive, and Q1 base current will stop. This cuts off Q1. With no current in the collector winding of the core, the current in the reset winding resets the core. This reset current is furnished to the reset winding (pins 4 and 5 of the core) through resistor R4 and diodes CR2 and CR4. This involves going from the plus saturation condition attained during the output pulse to a minus saturation condition (reset). During this time, the voltages at the feedback winding and the collector winding are reversed. The reversal of a voltage at the feedback winding increases the reverse bias on Q1. The reversal of voltage in the collector winding tends to drive the output voltage somewhat more positive than the +12 volts on pin 7. It takes approximately 30 microseconds for the reset action to be accomplished.

The amplifier section Q2 is normally biased to cutoff by voltage divider R7 and R6. With no collector current flowing, the quiescent collector voltage of Q2 is -20 volts. The negative going pulse generated by the blocking oscillator section is coupled to the amplifier base through CR3, R5, and C3. The diode provides for rapid cut off of the amplifier, thereby minimizing the fall time. R5 and C3 serve as base current limiting and rise time determinants. The load is connected between -20 volts and 0 volts and should be limited to no less than 8 ohms (20 to 24 MN11 cores).



NOTE:
ALL RESISTORS ½ WATT ±10%
UNLESS OTHERWISE NOTED.

Schematic,

TN130B Core Driver

Dwg. #A103S130B

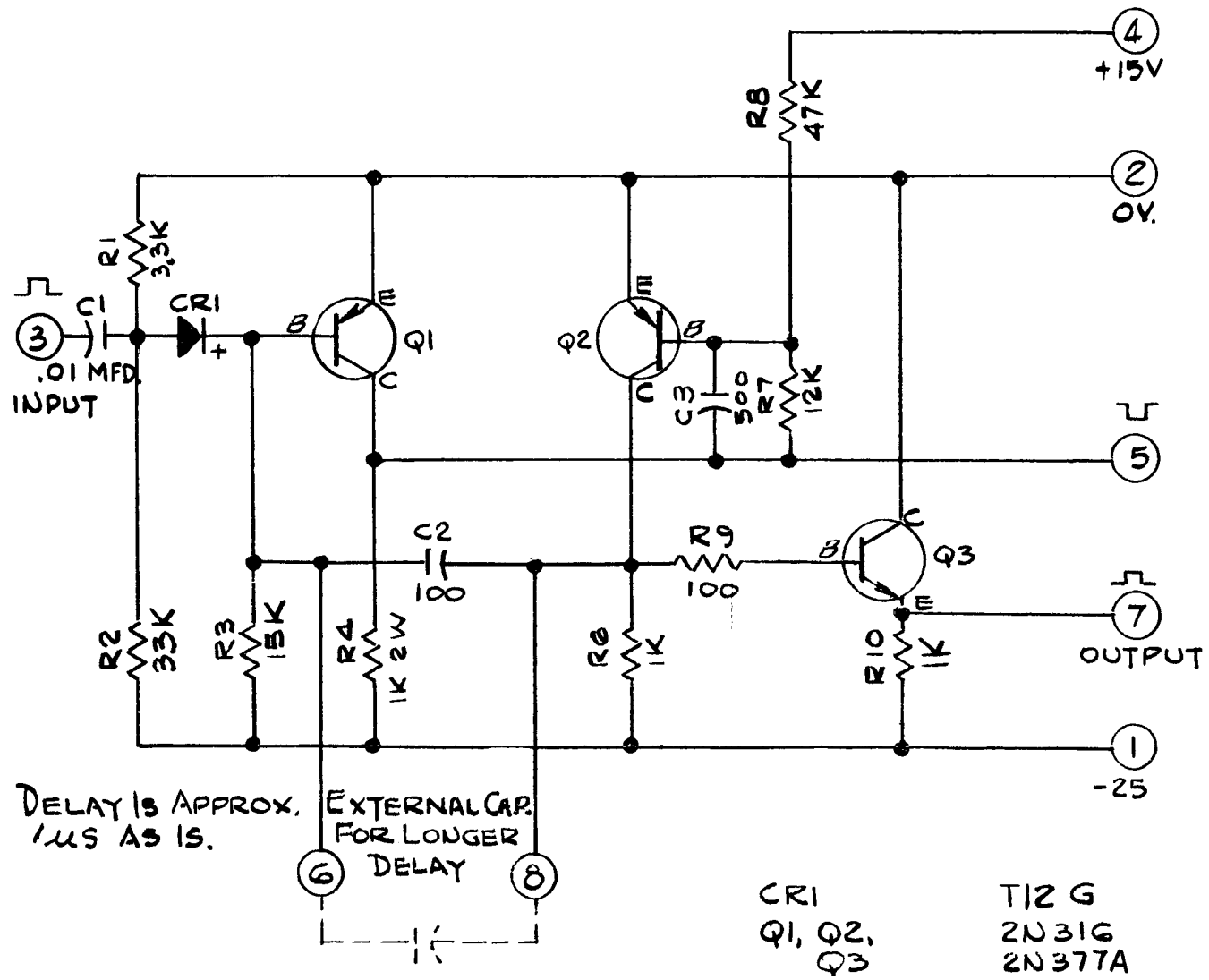
TN 138 B
ONE-SHOT WITH EMITTER FOLLOWER OUTPUT

The TN138B is a one-shot (monostable multivibrator) with an emitter follower output. This network can drive low impedance loads because of the emitter follower output.

The network's quiescent state is with Q1 saturated and with Q2 cut off. The base of Q1 is forward biased by R3 which is connected to -25 volts, thus saturating Q1. Since Q1 is saturated, the base of Q2 is reverse biased by the voltage divider R7 and R8 between +15 volts and the collector of Q1 (0 volts). With Q2 cut off, its collector is at approximately -25 volts; therefore the base of Q3 is at the same voltage as the emitter of Q3, keeping Q3 near cut off. Pin 7 will be at -25 volts and pin 5 will be at 0 volts. The resistor divider of R1 and R2 will maintain a reverse bias on diode CR1 of approximately 2.2 volts for protection against noise impulses. When a positive pulse of sufficient amplitude is applied to pin 3 to cause conduction of CR1, transistor Q1 will be cut off. The collector of Q1 will therefore go negative toward -25 volts. This negative going voltage potential is coupled to the base of Q2 through C3 and R7. This will cause the base of Q2 to go negative with respect to the emitter. Q2 will now conduct, and starts to saturate rapidly. The collector of Q2 will now go positive from -25 volts to 0 volts. This voltage change, being coupled through C2 to the base of Q1, will keep Q1 cut off after the input pulse has passed. C2 has now been charged, and will start to discharge through R3. When C2 has discharged sufficiently to allow the base of Q1 to return to its quiescent negative potential, Q1 will saturate. As Q1 saturates, its collector will go positive. Due to the resistor divider of R7 and R8, the base of Q2 will also go positive, reverse biasing Q2 and cutting it off. The one-shot has now returned to its quiescent condition.

The time constant of R3 and C2 determines the pulse width, which is about 1 microsecond. By adding external capacity across pins 6 and 8, the RC time constant is increased and thus the pulse width is increased. When Q2 is saturated, the base of Q3 will be positive in respect to the emitter, and this will cause Q3 to go into saturation. Pin 7, the output of the emitter follower, will go to 0 volts. Q3 will be in saturation as long as Q2 is in saturation. When Q2 is cut off, Q3 will be near cut off, and pin 7 will return to -25 volts.

Although the description of operation has been based on voltages of +15 volts and -25 volts, this network will operate equally on voltages of +10 volts and -15 volts.



Schematic,

TN138B One-Shot with Emitter Follower Output

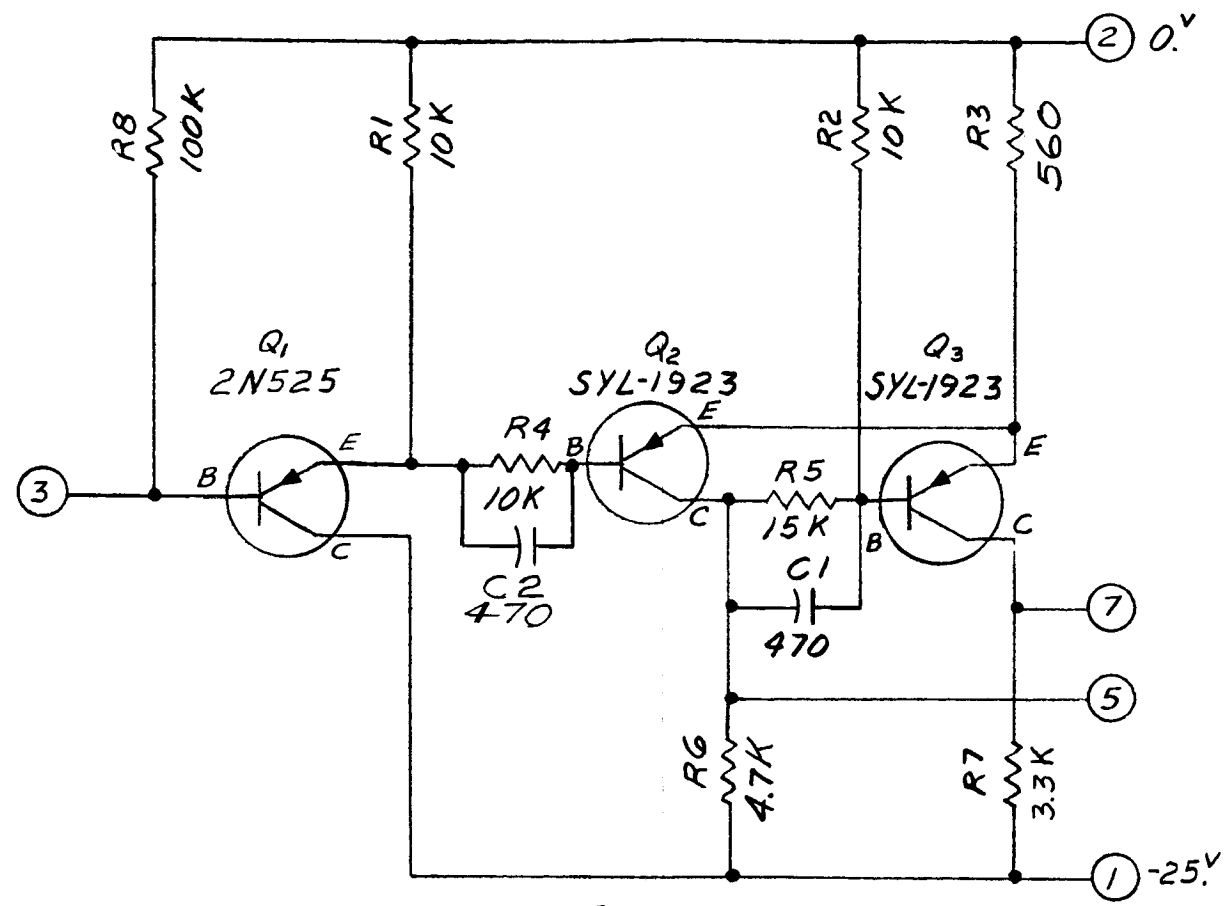
Dwg. #A103S138B

TN 150
SCHMITT TRIGGER

1. TN150 is a Schmitt trigger preceded by an emitter follower which presents an input impedance at approximately 70,000 ohms at pin #3. The circuit switches rapidly (in approximately 0.3 microseconds) from one state to the other with either a pulse or dc level change on pin #3 input. With the input disconnected or at a positive level, transistors Q1 and Q2 are cut-off and transistor Q3 is conducting.

2. Transistor Q1 is cut off by resistor R8 returning the base of Q1 to a more positive voltage than the emitter, and Q2 is cut-off by resistor R1 returning the base of Q2 to a more positive voltage than the emitter of Q2. The emitters of Q2 and transistor Q3 are at a negative voltage $-E_2$ developed by the current flow through resistor R3, Q3, and resistor R7. Transistor Q3 is conducting because the base is forward biased by the resistor divider consisting of resistors R2, R5, and R6; since Q2 is cut-off. When the input, pin #3, is taken to a negative voltage, Q1 is turned on, which makes the emitter of Q1 go negative (-25 volts). This will forward bias Q2, causing it to conduct. When Q2 is conducting, the base voltage of Q3 is raised to a more positive value than the emitter voltage, thus reversing the bias on Q3 and cutting it off. This causes the collector voltage of Q3 to go from approximately -3 volts to -25 volts. Capacitor C1 is used to speed up the switching time. The outputs, pin #7 and pin #5, are opposite polarity pulses from -25 volts to -3 volts. When the output is removed or goes positive, the circuit is returned to the original state.

3. Although the description of operation has been based on power supply voltages of -25 volts, this network will operate equally well on supply voltages down to -10 volts.



NOTE:
1. ALL RESISTORS $\frac{1}{2}$ WATT ±10% UNLESS OTHERWISE SPECIFIED.

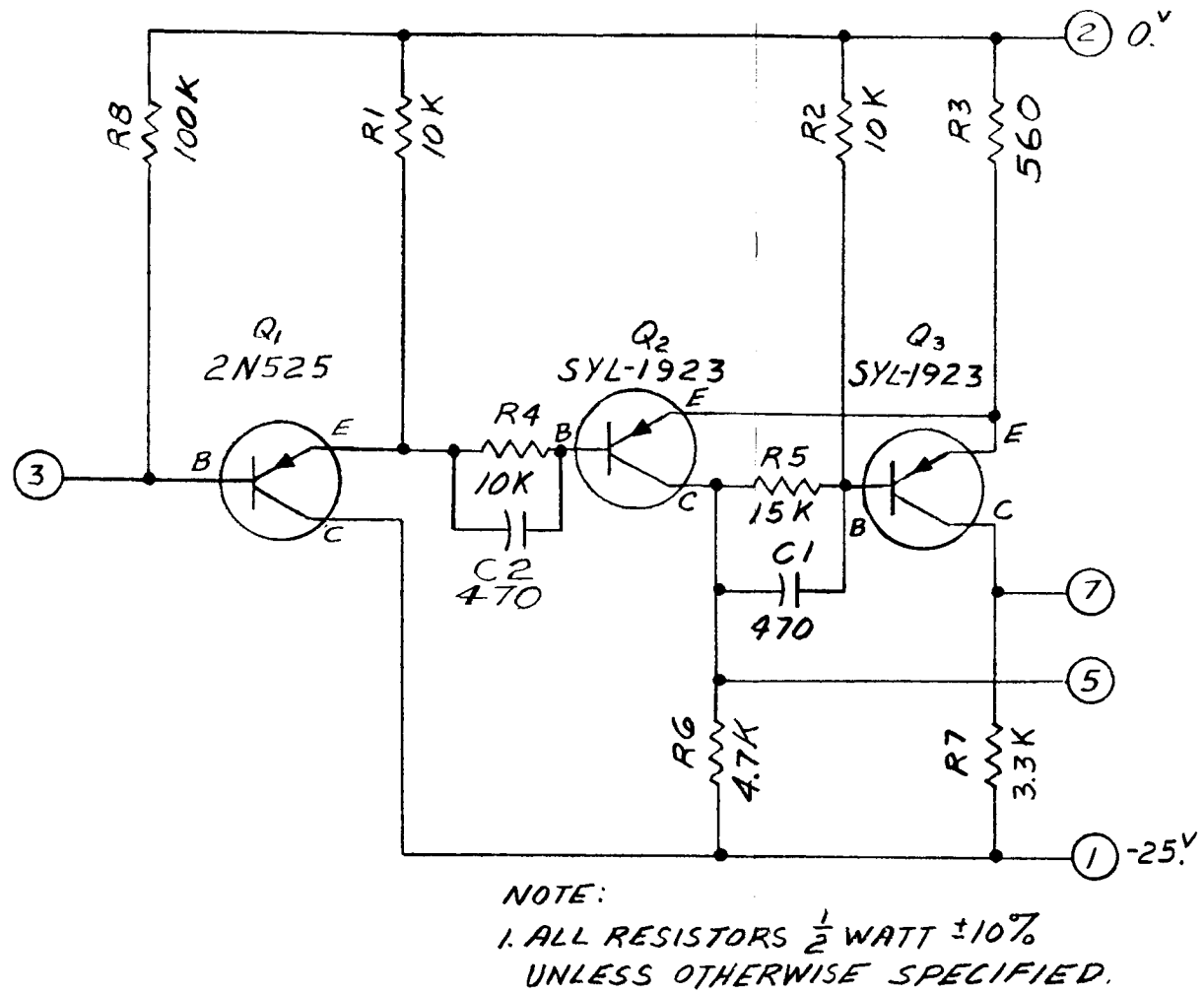
UNLESS OTHERWISE SPECIFIED:

1. Capacitance is in mmf.
2. Resistance is in ohms.

Schematic

TN-150 Schmitt Trigger

Dwg. #A103S150A



NOTE:
1. ALL RESISTORS $\frac{1}{2}$ WATT ±10% UNLESS OTHERWISE SPECIFIED.

Schematic,

TN150 Schmitt Trigger

Dwg. #A103S150A